SERVICE MANUAL
AT&T SYSTEM 75
MAINTENANCE SUPPORT

555-200-108IS
Issue 1, August 1984

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INTRODUCTION

This manual is a backup document for the *System Maintenance* manual (555-200-105IS). It includes information necessary to understand the overall system operation and to develop more complex trouble locating procedures than those covered in Manual 555-200-105IS.

ORGANIZATION

The information presented in this manual is divided into the following sections:

- **SWITCH HARDWARE**—Provides a functional description of the System 75 switch hardware. The switch hardware includes the switching network, switch processing element, high capacity minirecorder, applications processor interface, maintenance circuit pack, and power supply.
- **SYSTEM SOFTWARE** —Describes the system software resources including switched services software, administration software, and maintenance software.
- **TROUBLE CLEARING AIDS**—Describes the following trouble clearing aids:
  - — Alarm Log
  - — Error Log
  - — Maintenance Commands
  - — Facilities Access Test
- **ABBREVIATIONS AND ACRONYMS**
- **INDEX**

SWITCH HARDWARE

Figure 1 shows the System 75 switch. The basic switch hardware consists of the following:

- Switching network
- Switch processing element (SPE)
- High capacity minirecorder (HCMR)
- Applications processor (AP) interface
- Maintenance circuit pack
- Power system

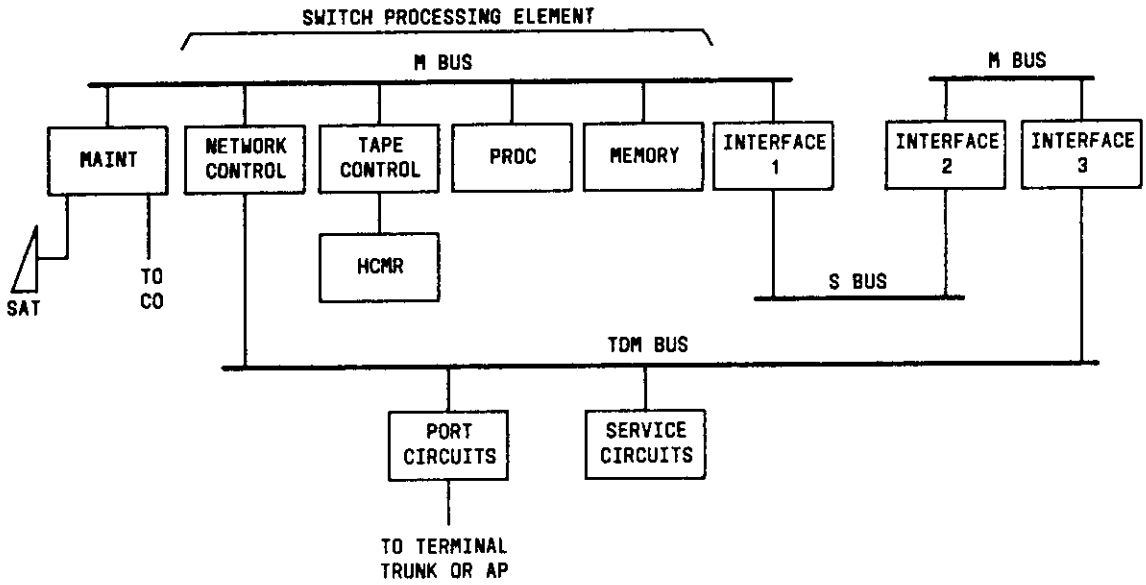

Figure 1. Communications Switch

SWITCHING NETWORK

System 75 uses distributed processing techniques to provide switched voice and data services. The switch operates at 64 Kbps. The switching network consists of the following:

- Time division multiplex (TDM) bus
- Intelligent ports
- Service circuits

The intelligent ports connect external communications facilities to the TDM bus. The TDM bus connects the intelligent ports to the SPE through the network control circuit. The service circuits provide tone sources, receivers, detectors, and pooled modems.

TDM Bus

Functional Description

The TDM bus consists of two groups of eight signals (A and B buses) and five control lines with matching grounds. The port circuit packs place digitized voice [pulse code modulated (PCM)] signals on the bus. Control channel information is carried on the bus in an 8-bit Control Channel Message Set (CCMS) data signal. The CCMS data signal allows the SPE to communicate with the port circuit packs.

The bus operates at 2.048 MHz. The system framing pulse is 8 kHz. This provides 256 time slots on both the A and B bus. The time slots are 488 ns wide. Time slots are generated as shown in Figure 2.

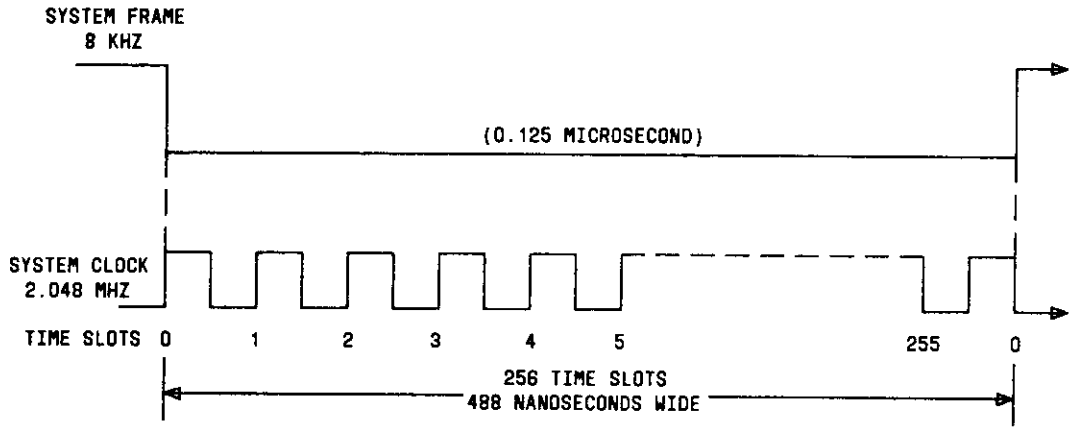

Figure 2. TDM Bus Time Slot Generation

Two time slots are required for a 2-party conversation. Each party transmits (talks) on one time slot and receives (listens) on another. The initial system software limits the number on a conference call to six. During a conference connection, each member of the conference transmits on an individual time slot while receiving on as many as five other time slots.

The actual switch capacity is 236 simultaneous conversations, because some slots are reserved for system use. The first five slots on Bus A (00—04) are used for the internal control channel on which the ports talk to the SPE. Seventeen slots on the B bus are used

for system tones (see Table A). Slots 05 through 12 on the A bus and slots 256 through 260 on the B bus are reserved for future use. The last two slots on each bus (254, 255, 510, and 511) are currently not used.

Physical Characteristics

The TDM bus contains two identical 8-bit buses (A and B). The TDM bus snakes continuously through several carriers within the cabinet as shown in Figure 3. The total length is about 15 feet for a system with four port carriers. The bus is driven from any of the circuit pack slots in the carriers. Similarly, a signal on the bus can be received by any circuit pack.

Within a carrier, the bus is printed on one side of the backplane while the other side is solid ground. Between carriers, coax cables are used to minimize electromagnetic interference (EMI).

Electrical Characteristics

The TDM bus is an unbalanced, low characteristic impedance transmission line. Paths printed over a ground plane on the carriers and the coax cables between carriers maintain this impedance level over the full length of the bus.

Each end of the bus is terminated to ground with a separate resistor for each of the 16 bits. Each circuit pack connects to the bus through a custom bus driver device. The bus driver is a switchable constant current source so that even in the "high" output state there is no bus loading to cause reflections. The current output of the drivers is adjusted so that logic "high" is 1.5 volts compared to a "low" of 0 volts.

TABLE A. Dedicated Time Slots For Tones

TDM-B Slot No.	Tone
261	697 Hz*
262	770 Hz*
263	852 Hz*
264	941 Hz*
265	1209 Hz*
266	1336 Hz*
267	1447 Hz*
268	1637 Hz*
269	Dial Tone
270	Re-order Tone
271	Intercept Tone
272	Busy Tone
273	Audible Alerting Tone
274	Special Audible Alerting Tone
275	2025 Hz
276	2225 Hz
277	Music

*These tones are used to generate touch-tone signals.

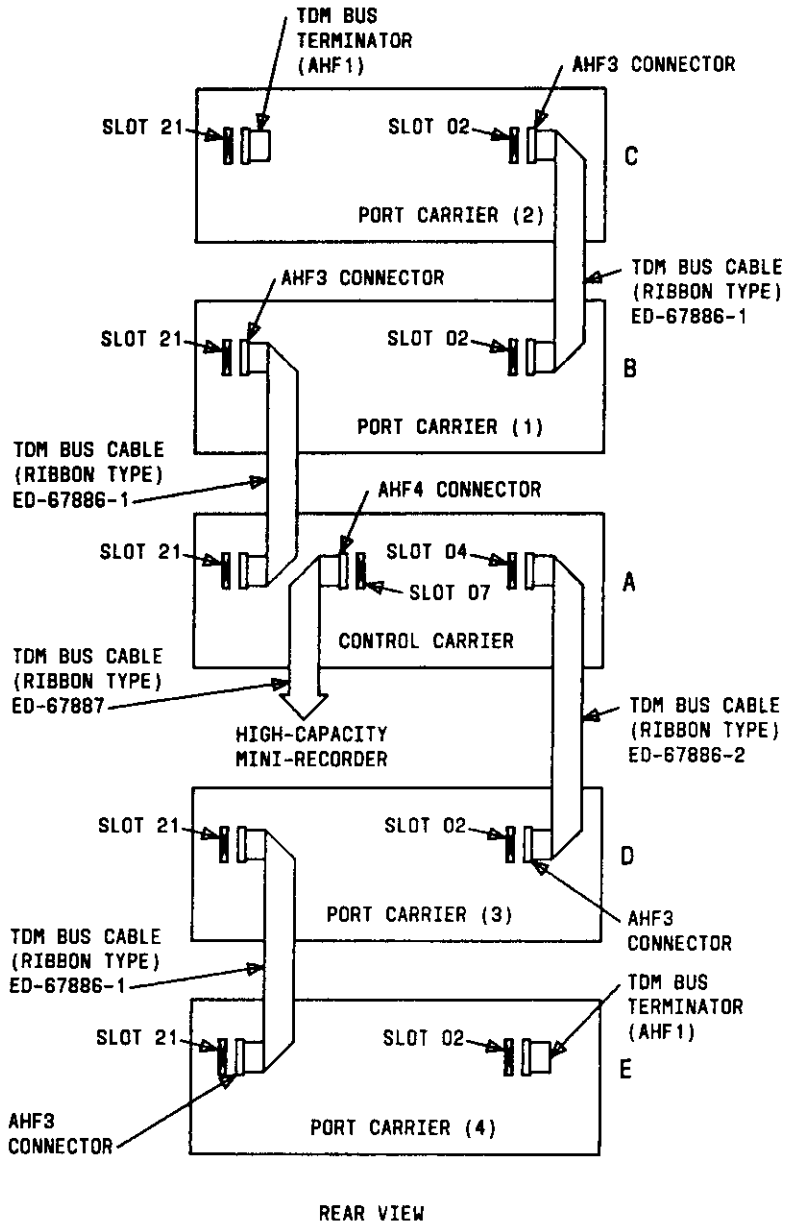

Figure 3. TDM Bus Wiring Diagram—Fully Loaded (4-Port Carrier and Control Carrier) Configuration

Intelligent Ports

Common Circuitry

The port circuit packs provide the link between trunks or terminals and the TDM buses. Eight port circuits are provided on most port circuit pack. The MET Line, Tie Trunk, and Auxiliary Trunk circuit packs contain four port circuits.

Each of the System 75 port circuit packs contain a number of common elements (see Figure 4) as well as the unique port circuits. The common elements are as follows:

- Bus buffers
- Sanity and control interface (SAKI)
- On-board microprocessor with external random access memory (RAM)
- Network processing elements (NPEs)

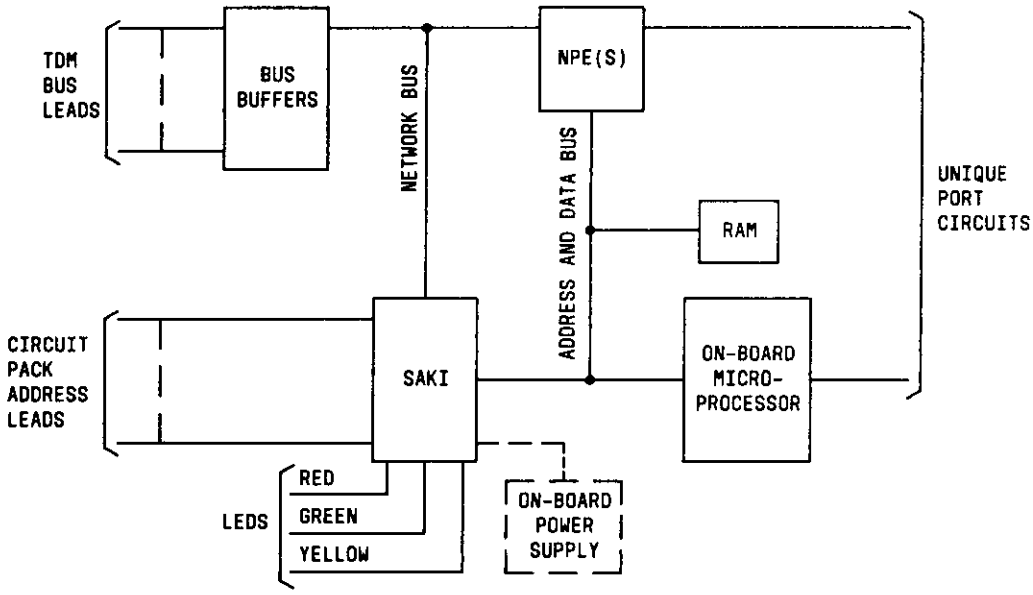

Figure 4. Port Circuit Pack Common Circuitry

Bus Buffers

The bus buffers are the digital interface between the backplane TDM bus wires (system bus) and the on-board circuitry (data bus). They receive or transmit on either of the two 8-bit TDM buses. They also receive and distribute clock and frame signals.

SAKI

The SAKI is the control interface between the SPE that sends information via the network control circuit down the TDM buses and the on-board circuitry controlled by the on-board microprocessor. The SAKI receives control information (down-link messages) on the first five time slots and, as requested by the on-board microprocessor, transmits control information (up-link messages) on these same time slots.

The SAKI also:

- Identifies the circuit pack to the SPE (location and vintage)
- Controls status indicator light-emitting diodes (LEDs)—red (failure), green (test), and yellow (circuit busy)
- Initiates power-on startup procedures
- Checks the on-board microprocessor for sanity and causes reinitialization in case of problems
- Takes NPEs out of service under control of the on-board microprocessor
- Resets the protocol handler on the Hybrid Line circuit pack and the formatter devices on the Digital Line circuit pack
- Takes the whole circuit pack out of service on command from the SPE or when it determines that on-board interference is present in the control time slots

On-Board Microprocessor With External RAM

The on-board processor performs all low level functions such as scanning for changes and relay operations. In general, it carries out commands received from the SPE and reports status changes to it. The external RAM stores control channel information and port-related information.

NPEs

Each port circuit pack contains one, two, or four NPEs. The Analog Line, Hybrid Line, CO Trunk, and DID Trunk circuit packs contain two NPEs. The Digital Line circuit pack contains four NPEs. The MET Line, Auxiliary Trunk, and Tie Trunk circuit packs contain one NPE.

The NPEs perform switching network functions for the port circuits. Under control of the on-board microprocessor, an NPE can connect a port circuit to any one of the TDM bus time slots. More specifically, it allows a port circuit to "talk" on one time slot and "listen" to the same time slot (NPE sidetone) and on up to five other time slots at the same time. In 2-wire circuits that provide their own sidetone, the NPE sidetone is not used.

Line Ports

Analog Line

The Analog Line circuit pack provides the electrical interface between eight analog voice terminal lines and the TDM bus. Figure 5 shows the following Analog Line unique circuitry:

- Ringing application circuit
- Port input/output (I/O) circuit
- Eight port circuits

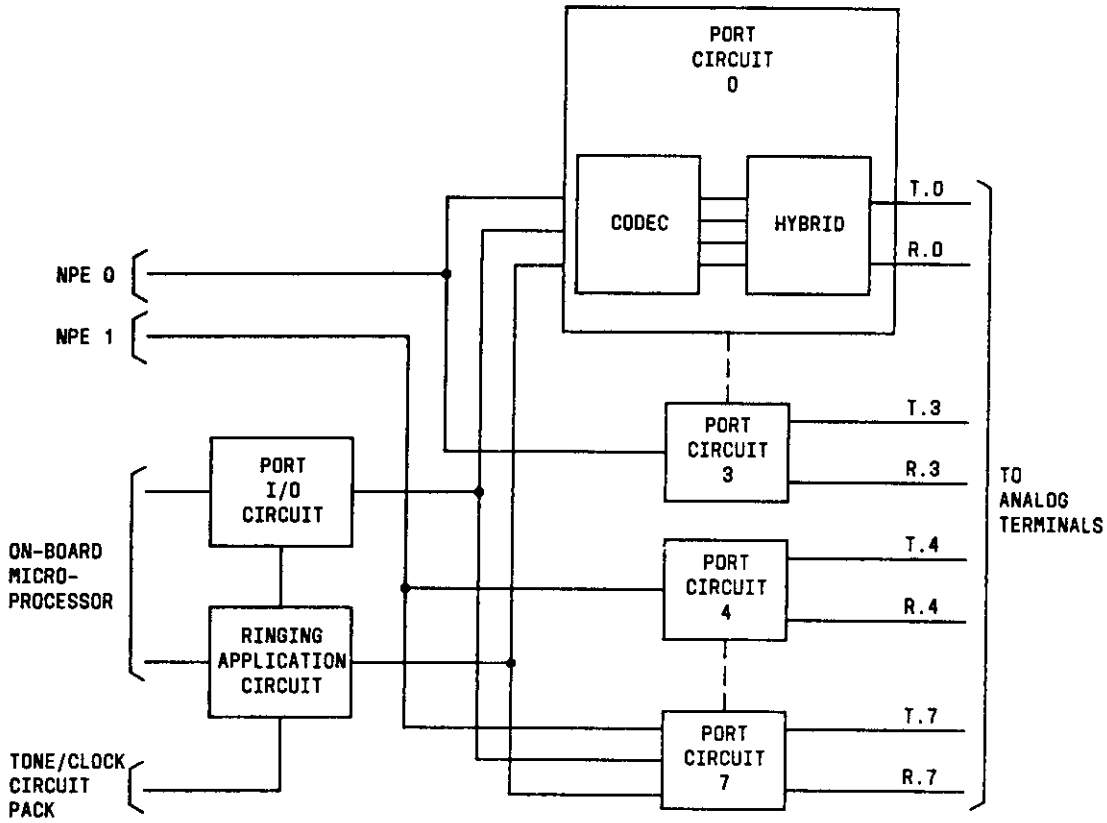

Figure 5. Unique Analog Line Circuitry

Ringing Application Circuit: This circuit receives ringing voltage from the 124B frequency generator located in the Power Distribution Unit. It monitors ringing voltage and current, generates signals to the on-board microprocessor indicating zero ringing voltage and current, and detects a terminal user lifting the receiver during ringing. This prevents the application of ringing to the port circuit when a terminal user lifts the receiver during the ringing phase. Maintenance circuitry is also included. The maintenance circuitry detects when a terminal is connected to the port circuitry and checks for faults in the ringing application circuitry.

Port I/O Circuit: This circuit consists of bus expanders for communication between the on-board microprocessor and the port circuits. It receives commands from the on-board microprocessor and distributes them to the individual port circuits. It also accesses the port circuit scan points and passes the information to the on-board microprocessor.

Port Circuits: The eight port circuits are identical. Each port circuit consists of a coder/decoder (codec), hybrid circuit, power filter, battery feed circuit, relay driver, and surge protection circuit.

The codec is a 4-wire circuit that converts the analog signal from a voice terminal to a PCM data signal. It converts an incoming PCM data signal from the NPEs to an analog signal. The hybrid circuit converts the 4-wire analog signal from the codec to a 2-wire analog signal that is connected to the analog line. Filtered power is provided for the codec and hybrid circuits.

The battery feed circuit provides talking battery to the voice terminal. It also produces a controlled dc battery feed for short and long loops, detects when a receiver is lifted, and provides the message waiting signal by periodically turning off the feed voltage.

The relay driver provides the interface between the ringing application circuit and the port circuit. It causes ringing turn on and turn off. The surge protection circuit provides lightning surge protection for the circuit pack.

Digital Line

The Digital Line circuit pack provides the electrical interface between eight digital communications protocol (DCP) lines and the TDM bus. Figure 6 shows the Digital Line unique circuitry. The unique circuitry consists of two formatter devices and eight port circuits.

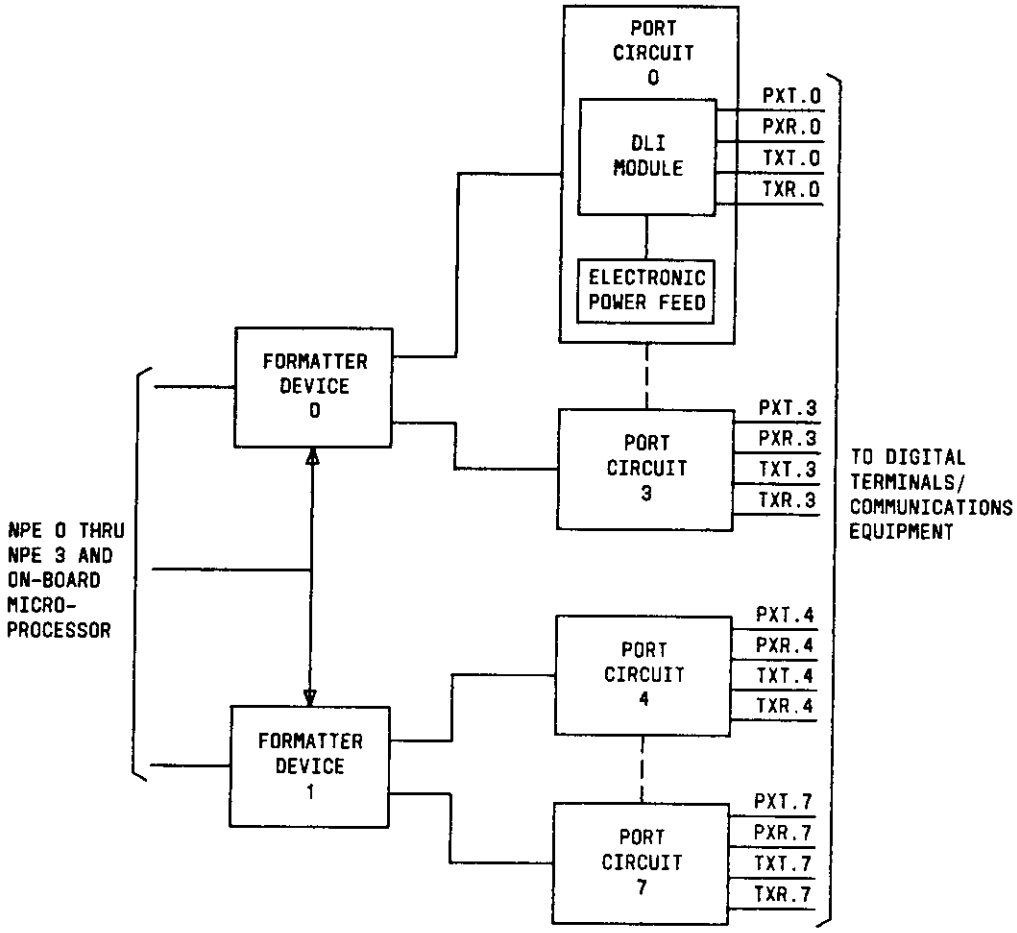

Figure 6. Unique Digital Line Circuitry

Formatter Devices: Each formatter device controls the format of control channel data for four DCP lines. The devices code control information from the on-board microprocessor, multiplex it with information from the NPE, and output it to the digital line interface (DLI) for transmission on the DCP line. Control information received from the DLI is stripped from the data stream, decoded, and forwarded to the on-board microprocessor.

Port Circuits: The eight port circuits are identical. Each port circuit consists of a DLI module and an electronic power feed device. The DLI module consists of a DLI device, a pair of interface devices, and two isolation transformers. The DLI device contains all functions needed to transmit and receive data over a DCP line. The transmitter function includes data

scrambling and band limit filtering. The receiver function includes equalization, clock recovery, data unscrambling, and frame detection. The two interface devices contain all discrete components (capacitors and resistors) needed to operate the DLI device correctly.

An isolation transformer is used for both the transmit and receive pair of the DCP line. Phantom power is supplied to the line (from the electronic power feed device) at the secondaries of the transformers. The primaries of the transformers connect to the DLI device.

The electronic power feed device supplies -48 volt dc phantom power to the line circuit. The electronic power feed device is a "smart" circuit breaker. When it senses an overcurrent condition, it indicates the condition on an output lead and goes into thermal shutdown if not turned off by the on-board microprocessor. When the overcurrent condition disappears, the circuit breaker can be turned on by the on-board microprocessor.

The electronic power feed device is polled regularly by the on-board microprocessor to test for overcurrent and no-current conditions. The polling can also occur upon demand.

Hybrid Line

The Hybrid Line circuit pack provides the electrical interface between eight hybrid voice terminals and the TDM bus. It terminates three pairs of wires from each terminal: analog voice pair, digital control pair, and power pair. Figure 7 shows the following Hybrid Line unique circuitry:

- Protocol handler
- Port I/O circuit
- Eight port circuits

Protocol Handler: The 8-bit on-board microprocessor translates the control information in CCMS message format to the control information message format used by the hybrid terminals. The protocol handler sends the messages to the terminals via transceivers located in the port circuits.

Port I/O Circuit: The port I/O circuit consists of a bus expander for communication between the on-board microprocessor and the port circuits. Half of the expander controls the on/off state of the electronic power feed devices located in the port circuits. The other half controls the balance in the hybrid circuit located in the analog port circuit.

Port Circuits: The eight port circuits are identical. Each port circuit consists of an analog port, one-half of a transceiver, and an electronic power feed device.

The analog port circuit consists of a codec, a hybrid circuit, an isolation transformer, and associated power filtering circuitry. The codec and hybrid circuit function the same as the codec and hybrid circuit in the Analog Line circuit pack. A lead from the port I/O to the hybrid circuit controls the terminating impedance of the hybrid circuit for testing purposes. The output of the hybrid circuit is connected to the primary of the isolation transformer. The secondary of the transformer is connected to the talking tip and ring pair with associated matching resistor.

The transceiver interfaces the control pair from the voice terminal to the protocol handler. The electronic power feed device provides -48 volts dc on the power pair to the voice terminal. The -48 volt dc input to the device is received through a fuse on the circuit pack. The device is polled by the on-board microprocessor, periodically and on demand, to test for an overcurrent and/or no-current condition. The on/off state of the device is controlled by the on-board microprocessor through the port I/O circuit.

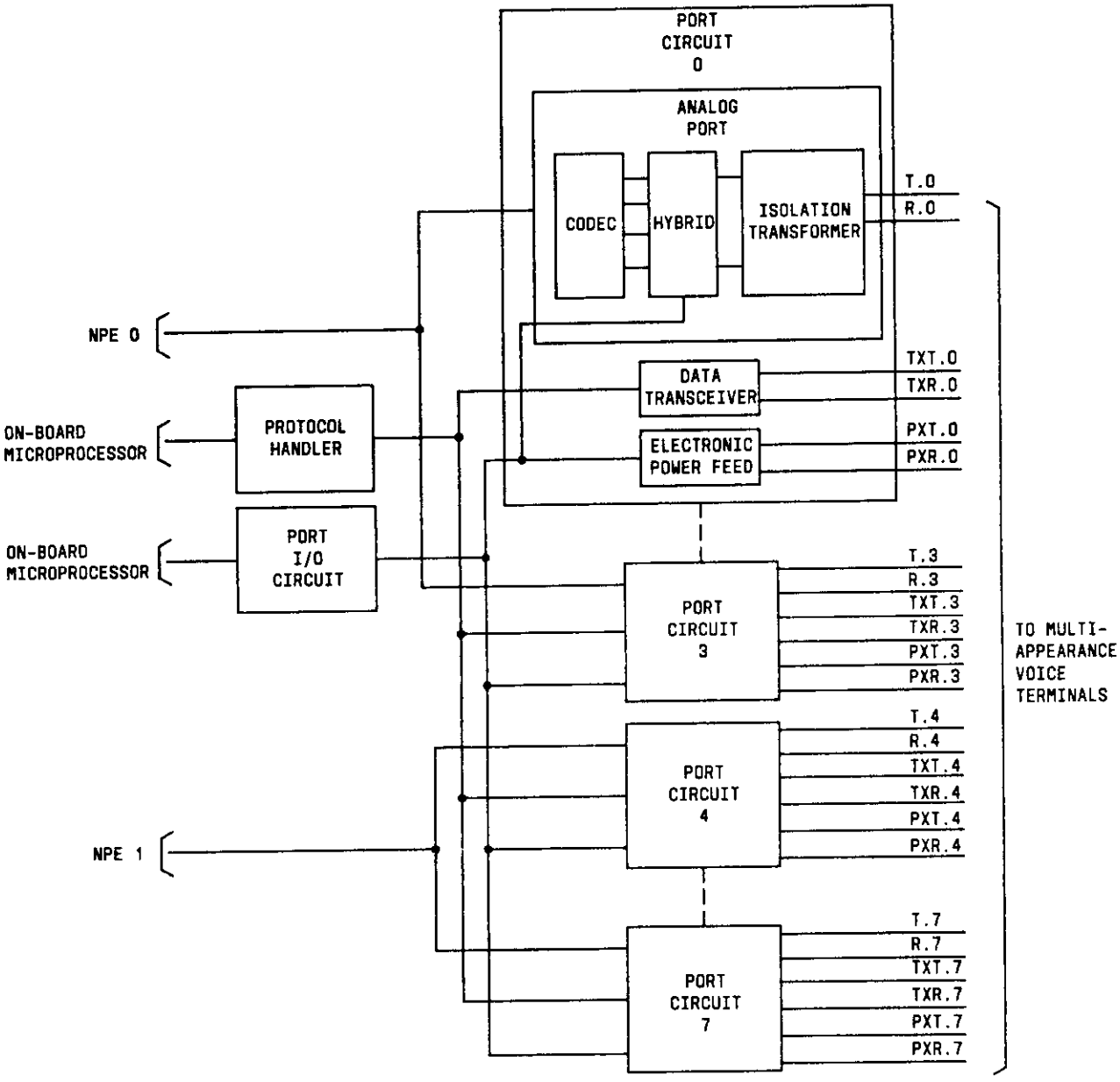

Figure 7. Unique Hybrid Line Circuitry

MET Line

The MET line provides the interface between four multibutton electronic telephone (MET) lines and the TDM bus. Figure 8 shows the MET line unique circuitry. The unique circuitry consists of four port circuits.

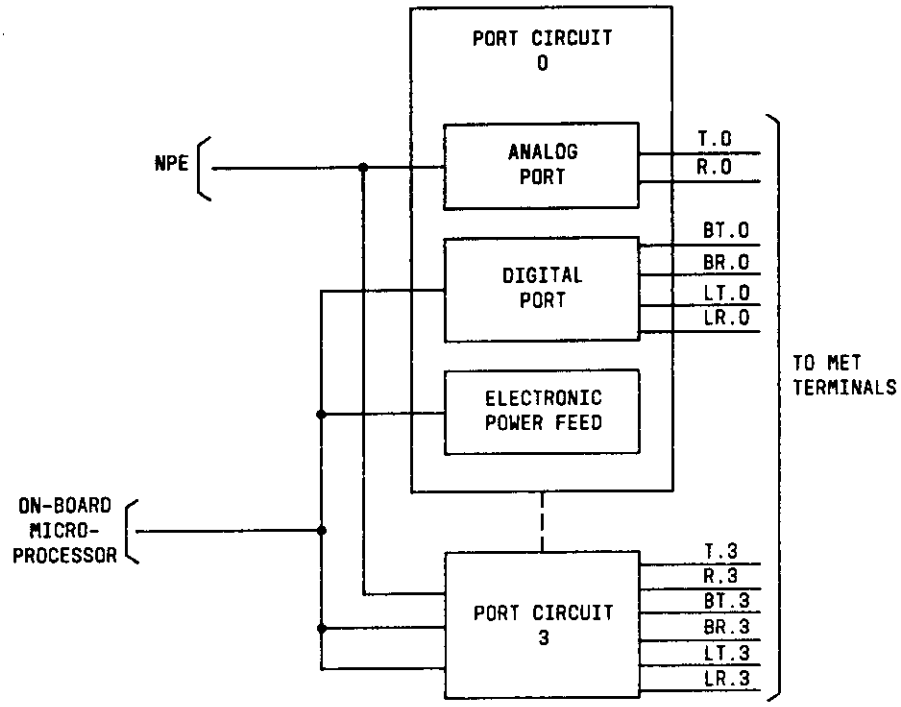

Figure 8. Unique MET Line Circuitry

Port Circuits: The four port circuits are identical. Each port circuit consists of an analog port, a digital port, and an electronic power feed device.

The analog port circuit consists of a codec, a hybrid circuit, an electronic battery feed, and a power filter. The codec, hybrid circuit, and power filter function the same as in the Analog Line circuit pack. The electronic battery feed provides talking battery to the MET set. The electronic battery feed produces a controlled dc battery feed current for short and long loops and detects when a MET set user lifts a receiver.

The digital port circuit provides a full duplex channel over two 2-wire pairs. All outgoing lamp and incoming button depression information is carried on these channels. Ringing and detection of when a MET set user lifts a receiver information is also sent over these channels.

The electronic power feed device provides phantomed -48 volt dc power for the MET terminals over the data channels. The electronic power feed device is a "smart" circuit breaker. When it senses an overcurrent condition, it indicates the condition on an output lead and goes into thermal shutdown if not turned off by the on-board microprocessor. When the overcurrent condition disappears, the circuit breaker can be turned on by the on-board microprocessor.

Trunk Ports

CO Trunk

The CO Trunk circuit pack provides the electrical interface between eight central office trunks and the TDM bus. Figure 9 shows the following CO Trunk unique circuitry:

- Ground detector circuit
- Port input/output (I/O) circuit
- Eight port circuits

Ground Detector Circuit: The ground detector circuit determines whether ground has been applied to the tip lead (incoming or outgoing seizure). One ground sensor is used for each port circuit. Input for the ground sensor comes from the port circuit as an analog current to the -48 volt dc supply. The ground sensor's output is a port control point to the port I/O circuit.

Port I/O Circuit: This circuit functions the same as in the Analog Line port I/O circuit.

Port Circuits: The eight port circuits are identical. Each port circuit consists of a codec, hybrid circuit, line transformer, power filter, relay driver, and surge protection circuit.

The codec is a 4-wire circuit that converts an incoming PCM data signal from a system user (via the NPEs) to an analog signal. It converts the analog signal from a central office trunk to a PCM data signal. The hybrid circuit converts the 4-wire analog signal from the codec to a 2-wire analog signal that is connected to the central office trunk by the line transformer. Filtered power is provided for the codec and hybrid circuits.

The relay driver buffers and inverts the relay drive signals from the port I/O circuit so that a logic high input operates the appropriate relay. The relays control circuitry that provides the proper interfaces for ground start or loop start trunks and rotary or touch-tone dialing. The surge protection circuit provides lightning surge protection for the circuit pack.

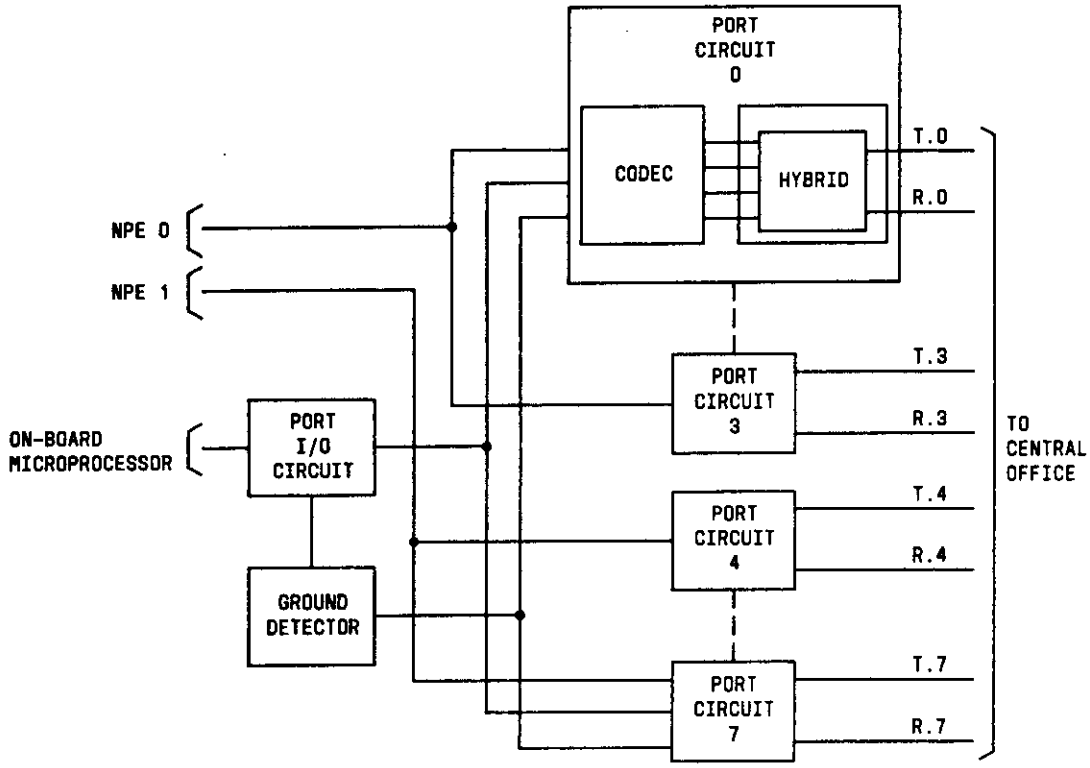

Figure 9. Unique CO Trunk Circuitry

DID Trunk

The DID Trunk circuit pack provides the electrical interface between eight central office trunks arranged for direct inward dialing (DID) and the TDM bus. Figure 10 shows the DID Trunk unique circuitry. The unique circuitry consists of a port input/output (I/O) circuit and eight port circuits.

Port I/O Circuit: This circuit functions the same as in the Analog Line port I/O circuit.

Port Circuits: The eight port circuits are identical. Each port circuit consists of a codec, balance network, trunk interface unit, loop termination circuit, and power filter.

The codec is a 4-wire circuit that converts the analog signal from a DID trunk to a PCM data signal. The codec converts an incoming PCM data signal from the NPEs to an analog signal.

The trunk interface unit contains a hybrid, a 2-wire interface circuit, and control circuitry. The hybrid circuit converts the 4-wire analog signal from the codec to a 2-wire analog signal that is connected to the analog line by the 2-wire interface circuit. The control circuitry controls loop current, internal signal gain, terminating resistance, battery feed shutdown, and battery reversal.

The loop termination circuit provides a fixed impedance to the DID trunk. Filtered power is provided for the codec and hybrid circuits.

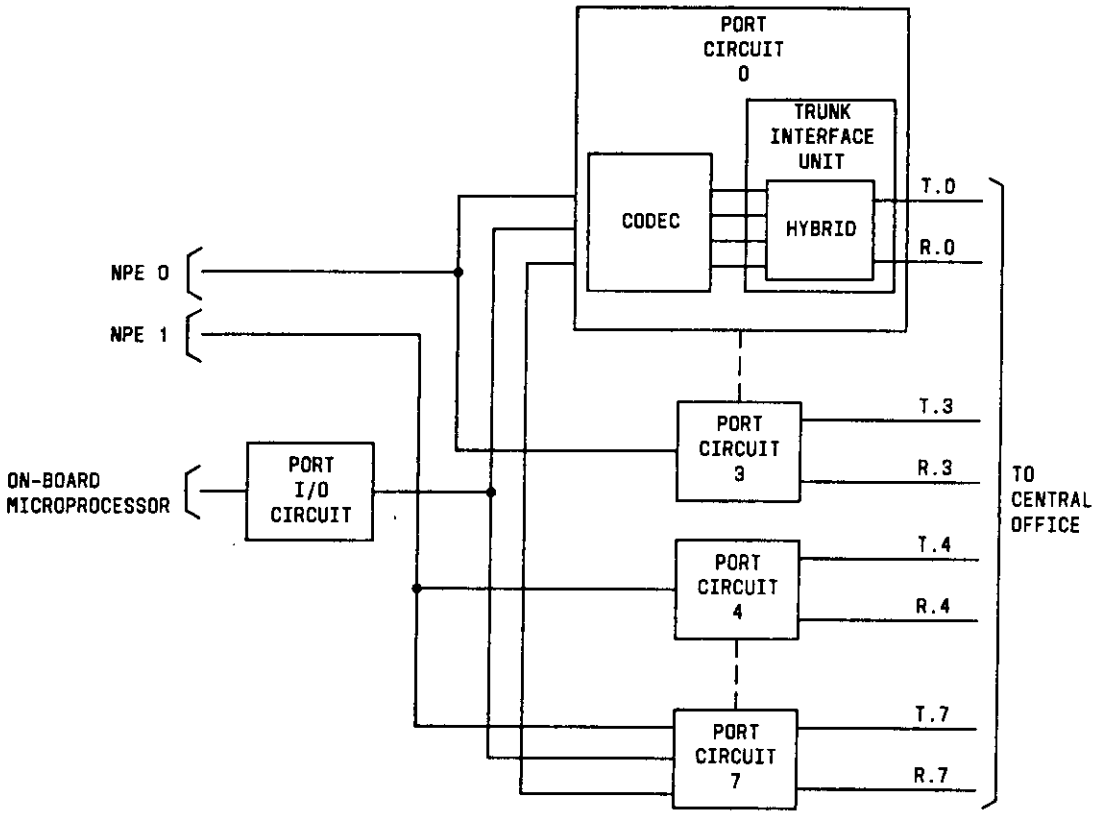

Figure 10. Unique DID Trunk Circuitry

Tie Trunk

The Tie Trunk circuit pack provides the electrical interface between four 6-wire tie trunks and the TDM bus. Two tip and ring pairs form a 4-wire analog transmission line. The E and M pair are used for signaling. The T and R pair transmit analog signals from the circuit pack. The T1 and R1 pair receive analog signals from the tie trunk. The E and M pair are dc signaling leads used for call setup handshaking. The E lead receives signals from the tie trunk and the M lead provides signals from the circuit pack. Figure 11 shows the following Tie Trunk unique circuitry:

- Ground detector circuit
- Port I/O circuit
- Four port circuits

Ground Detector Circuit: This circuit determines if a ground has been applied to the E lead. Ground detector inputs come from the port circuits as an analog current to the -48 volt dc supply. Its output is a port control point to the port I/O circuit.

Port I/O Circuit: This circuit functions the same as in the Analog Line port I/O circuit.

Port Circuits: The port circuits are identical, except for port 3 where part of the E-lead maintenance circuit is located. Each port circuit consists of a codec with associated input and output line transformers, analog operational amplifiers, a power filter, loop-around transistors, port control comparators, a relay driver, an electronic power feed device, an E-lead test maintenance circuit, and surge protection circuits.

The codec converts the incoming 4-wire analog signal from the tie trunk to a PCM data signal. The codec converts the incoming PCM data signal from the NPE to an analog signal. Outgoing and incoming line transformers provide dc isolation to the tip and ring leads. Analog operational amplifiers provide amplification and buffering for the codec and network and loop-around gain compensation. Filtered power is provided to the codec and amplifiers.

The loop-around transistors are under control of the port control comparators and provide a loop-around path for the analog signal for testing purposes. The relay driver buffers and inverts the relay drive signals from the port I/O circuit so that a logic high input operates the appropriate relay. The relays and electronic power feed device control the M-lead circuitry to provide the proper signaling handshake for call progress trunks and rotary dialing.

The electronic feed device provides a -48 volt dc current to the M-lead circuits. It also tests the M-lead circuits for opens or shorts and prevents uncontrolled operation during power-up. The E-lead test circuit provides a ground to the ground detector circuit for testing purposes. The surge protection circuitry provides lightning surge and power cross protection for the circuit pack.

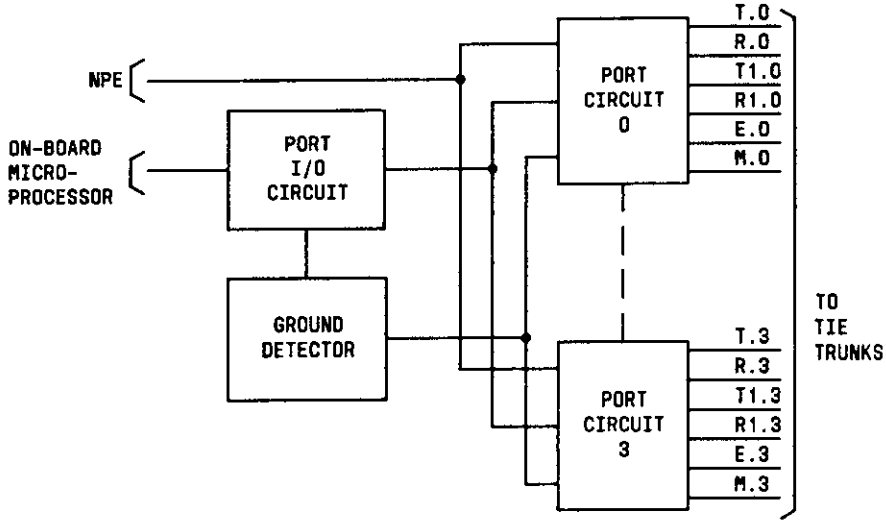

Figure 11. Unique Tie Trunk Circuitry

Auxiliary Trunk

The Auxiliary Trunk circuit pack provides the electrical interface between four ports provided for client-provided equipment (CPE) and the TDM bus. It is connected to the CPE by up to three pairs of wires. The transmission pair (T and R) carry voice signals and touch-tone control signals. T and R also provide a loop start seizure indication to the CPE. The seizure pair (SZ and SZ1) provide seizure indication to the CPE. The signal pair (S and S1) provide answer supervision and/or make-busy information from the CPE. Depending on the application, the transmission pair only or all three pairs are connected to the CPE.

Figure 12 shows the following Auxiliary Trunk unique circuitry:

- Ground detector circuit
- Port input/output (I/O) circuit
- Four port circuits

Ground Detector Circuit: This circuit determines if an answer-supervision or make-busy signal from the CPE is present. The ground detector's inputs come from the port circuits as an analog current to the -48 volt dc supply. Its output is a port control point to the port I/O circuit.

Port I/O Circuit: This circuit functions the same as in the Analog Line port I/O circuit.

Port Circuits: The four port circuits are identical. Each port circuit consists of a codec, hybrid circuit, line transformer, power filter, relay driver, battery polarity sensor, and surge protection circuit.

The codec is a 4-wire circuit that converts the analog signal from the CPE to a PCM data signal. It converts an incoming PCM data signal from the NPE to an analog signal. The hybrid circuit converts the 4-wire analog signal from the codec to a 2-wire analog signal that is connected to the CPE by a line transformer. Filtered power is provided for the codec and hybrid circuits.

The relay driver buffers and inverts the relay drive signals from the port I/O circuit so that a logic high input operates the appropriate relay. The relays control circuitry that provide the proper interfaces for CPE and rotary dialing.

The surge protection circuit provides metallic lightning surge protection for the circuit pack. Longitudinal surges are isolated from the hybrid and codec by the line transformer.

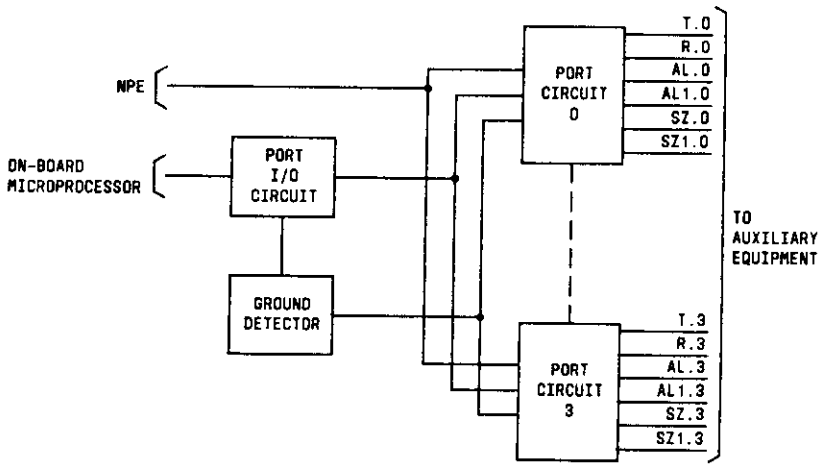

Figure 12. Unique Auxiliary Trunk Circuitry

Service Circuits

Tone/Clock

The Tone/Clock circuit pack provides clock signals to run the system and system call tones. The Tone/Clock circuit pack consists of the following (see Figure 13):

- Bus buffers
- Sanity and control interface (SAKI)
- On-board microprocessor with external RAM
- Clock circuit
- Tone Generator
- Time slot table and counter

Each system contains one Tone/Clock circuit pack. Power for the circuit pack (+5 volts dc) is provided on the backplane.

Bus Buffers: There are three bus buffers on the Tone/Clock circuit pack. The clock driver/receiver interfaces the three system clock signals (2.048 MHz, 8 kHz, and 160 kHz) to the TDM bus. Bus buffer A interfaces messages to and from the SPE on TDM bus A to the Tone/Clock circuit pack. Bus buffer B interfaces the system tones (see Table A) from the circuit pack to TDM bus B. Music is not produced by the Tone/Clock circuit pack. Music is provided by CPE through the Auxiliary Trunk circuit pack.

These tones are programmed to be placed on bus A when the circuit pack is first powered up. A downlink message from the SPE causes the tones to be switched to bus B.

SAKI: This circuit functions the same as in the SAKI in the common circuitry for the intelligent port circuits.

On-Board Microprocessor With External RAM: This circuit functions the same as the microprocessor in the common circuitry for the intelligent port circuits. In addition, it tells the dual-port RAM in the time slot table circuit the appropriate time slots to place the tones. The external RAM also has work space for complex tones.

Clock Circuit: The clock circuit consists of a 20.48-MHz oscillator, a clock generator, and a tone clock. The clock circuit runs independent from the rest of the Tone/Clock circuitry. The clock circuits start running when the circuit pack is first powered up and is not controlled by the on-board microprocessor.

The output of the 20.48-MHz oscillator is fed to the clock generator. The clock generator contains circuits that divide by 10, 2560, and 128. These circuits produce the 2.048-MHz, 8-kHz, and 160-kHz clock signals, respectively. The clock generator feeds these signals to the clock driver/receiver bus buffer and the tone clock. The tone clock uses these signals to synchronize the counters in the tone generator and time slot table circuits to the TDM bus.

Tone Generator: The tone generator consists of two digital signal processors (DSPs), a counter, and a dual-port tone RAM. The DSPs operate at 8 MHz and produces 32 different tones. The dual-port tone RAM stores these tones in 32 different addresses. The counter under control of the tone clock causes the DSPs to transmit one sample of each tone every 8-kHz. The counter is synchronized to the TDM bus and is offset to provide delay needed for access time.

Time Slot Table: The time slot table consists of a dual-port time slot table RAM and a counter. The dual-port RAM contains 256 different addresses. These addresses correspond to the time slots on TDM bus B. The counter sequences through the time slot table addresses in the dual-port RAM and causes the proper tone(s) to be output by the dual-port tone RAM on TDM bus B time slots.

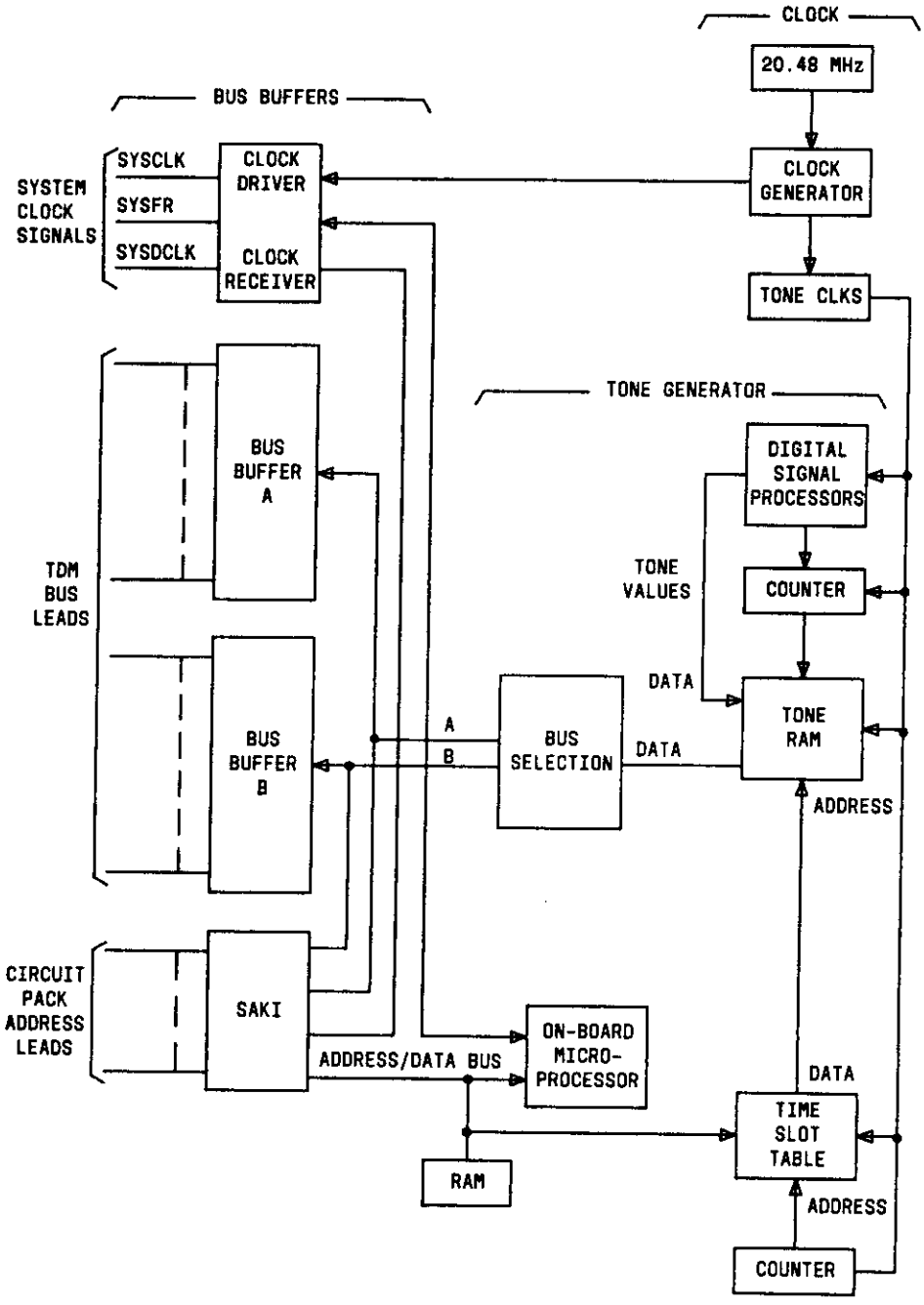

Figure 13. Tone/Clock Circuit

Tone Detector

The Tone Detector circuit pack provides four touch-tone receivers and two general purpose tone receivers that detect the appropriate system and network tones on the TDM bus.

The Tone Detector circuit pack consists of the same common circuitry as the intelligent port circuits and the following unique circuits (see Figure 14):

- Port I/O circuit
- Port or DSP Sanity check circuit
- Eight port circuits

Common Circuitry: The Tone Detector circuit pack common circuitry functions the same as the port circuits common circuitry.

Port I/O and Sanity Check Circuit: This circuit interfaces the on-board microprocessor to the port circuits and checks the sanity status of the port circuits' DSPs.

Port Circuits: There are eight port circuits. Each port circuit is connected to a network processing element (NPE) serial input and serial output. Port circuits 0, 1, 4, and 5 are touch-tone ports. Port circuits 2 and 4 are general purpose tone detector ports. Each of the six port circuits has an associated DSP. The remaining port circuits (3 and 7) provide a loop-around path for testing purposes and are tied directly with no associated circuitry to an NPE.

The two general purpose tone detector port circuits are identical and detect the following:

- Call-progress tones
- Modem answer-back tones
- Transmission test tones
- Noise

The four touch-tone tone detector port circuits are also identical. They detect touch-tone signals required for proper signaling.

The six port circuits used for tone detection contain a DSP, NPE to DSP interface circuitry, and a DSP restart circuit. The touch-tone port circuit also contains an interrupt filter. The general purpose tone detector port circuit will support an add-on emulator circuit for future changes in its DSP operating program.

TDM bus signals are connected to the DSP in serial form from the NPEs by the DSP interface circuit. Serial clock and data signals connect directly from the NPE to the DSP. The system framing signal is synchronized and connects to the DSP.

The DSP restart circuit controls the DSPs. When the on-board microprocessor is not functioning properly, the DSP restart circuit takes all of the DSPs out of service. It restarts each individual DSP under control of the port I/O and sanity check circuit. It resets the general purpose tone detector DSP after each use.

The two types of DSPs (general purpose tone detector and touch-tone) differ in internal programming and running speed. The touch-tone DSPs, under control of the on-board microprocessor, write data synchronously to the NPEs. The interrupt filter detects valid touch-tone signals and allows end-to-end transmission while blocking end-to-end touch-tone signaling. The general purpose tone detector DSPs, under control of the on-board microprocessor, write data asynchronously to the NPEs.

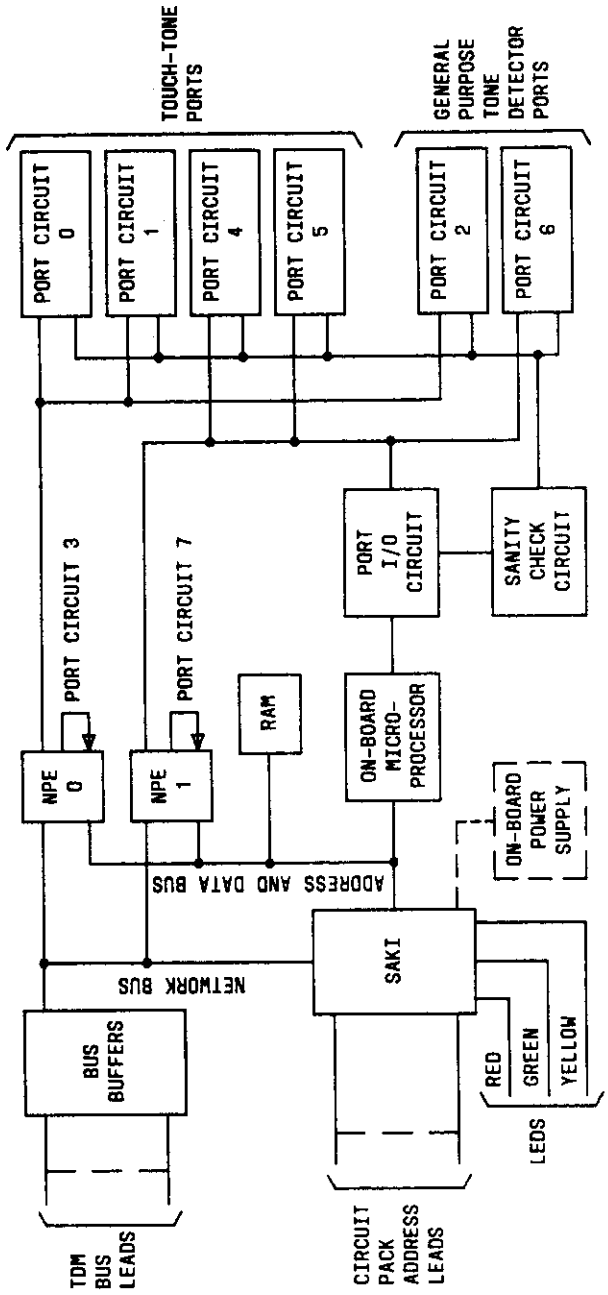

Figure 14. Tone Detector Circuit

Pooled Modem

The Pooled Modem circuit pack supports 0—300 and 1200 bits per second (bps) data speeds and provides the following:

- Circuitry to convert a DCP, Mode 2 signal into a signal compatible with the modulation formats of the 212-series modems
- Modem emulation (See below)

Capability	Data Module Mode
0—300 Asynchronous	Low
300 Asynchronous	300 Asynchronous
1200 Asynchronous	1200 Asynchronous
1200 Synchronous	1200 Synchronous

- Several modem functions appropriate to 212-series modem operations

A maximum of 16 Pooled Modem circuit packs are allowed in a system.

The Pooled Modem circuit pack consists of common circuitry and two conversion resources (see Figure 15). The conversion resource (port) enables two dissimilar devices to talk to each other. Each port has two connections to the TDM bus. One connection is made to a remote data module, DCP Mode 2 format. The other connection is made to a remote mode, PCM signal.

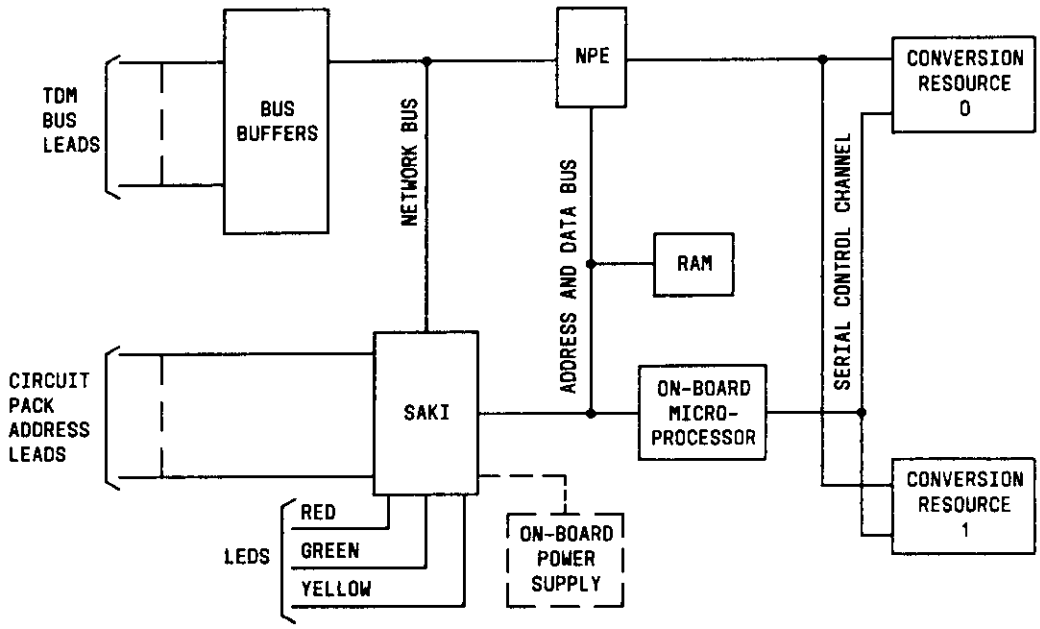

Figure 15. Pooled Modem Circuit

Common Circuitry: The Pooled Modem common circuitry provides the same general function as the intelligent port common circuitry.

Conversion Resources: The two conversion resources (port circuits) are identical and each contain the following:

- Microprocessor
- Transmit and receive I-channel controller (TRIC)
- Universal synchronous/asynchronous receiver and transmitter (USART)
- Data USART clock (DUCK)
- DSP

The port circuit microprocessor enables communications between a remote data module and a remote modem through control of an on-board data module and modem. The port circuit microprocessor communicates with the on-board microprocessor over a serial control channel. This channel allows the on-board microprocessor to send messages to the port circuit microprocessor that specify call startup information, option settings, information requests, various test modes, and call termination information. It also allows the port circuit microprocessor to inform the on-board microprocessor of various port circuit status information.

The DUCK and TRIC interface the I-channel information between the port circuit and the remote data module. The port circuit microprocessor controls the operation of the DUCK and the TRIC by appropriately programming their internal registers. The DUCK and TRIC together recreate the clock and serial data stream from the remote data module, and process an on-board clock and serial data stream for delivery to the remote data module. Control information (handshaking and RS232 control leads) is passed between the port circuit microprocessor and the remote data module by the TRIC.

The USART interfaces the DUCK's serial data stream to the port circuit microprocessor. The USART can be programmed by the port circuit microprocessor to operate synchronously or asynchronously. The USART also performs the following tasks for the port circuit microprocessor:

- Appends start and stop bits to parallel data received from the port circuit microprocessor in the asynchronous mode
- Converts serial data received from the port circuit microprocessor to parallel data and converts serial data received from the DUCK to parallel data
- Double buffers data in both directions
- Detects and generates break characters

The DSP provides modem emulation. It interfaces the port circuit PCM signal and the remote modem. PCM samples are communicated between the DSP and an analog line or trunk circuit connected directly or indirectly to the remote modem. The port circuit microprocessor directs the DSP to execute one of many programs. The DSP produces data, carrier detection, and timing information for the port circuit microprocessor. It accepts data and timing information from the port circuit microprocessor in a format dependent on its operating mode.

SWITCH PROCESSING ELEMENT

The main components of the switch processing element (SPE) are as follows (see Figure 1).

- Network Control
- Processor
- Memory
- Tape Control

These four components are interconnected by the 16-bit, 2-MHz M (memory) bus located on the backplane. The M bus also contains 24 address, 5 parity, and 10 interrupt and control lines.

The Maintenance circuit pack is associated with the SPE on the same M bus. The AP interface circuit packs are also associated with the SPE via the M bus, the S (system) bus, and an identical but shorter M bus.

Network Control

The Network Control circuit pack functions as follows:

- Synchronizes control channel messages between the switch processing element (SPE) over the M bus and the port circuits over the TDM bus
- Provides switched data access to the SPE for system administration, station message detail recording (SMDR), and switch maintenance
- Provides the time, day, and month to the SPE with battery holdover
- Monitors system clocks

Each system contains one Network Control circuit pack. Power for the circuit pack (+5 volts dc) is provided on the backplane.

The Network Control circuit pack consists of the following circuitry (see Figure 16):

- 8-bit on-board microprocessor A with external RAM and associated network interface circuitry
- 8-bit on-board microprocessor B with external RAM and associated network interface circuitry
- Two scanner circuits
- Clock circuit
- M bus interface circuit

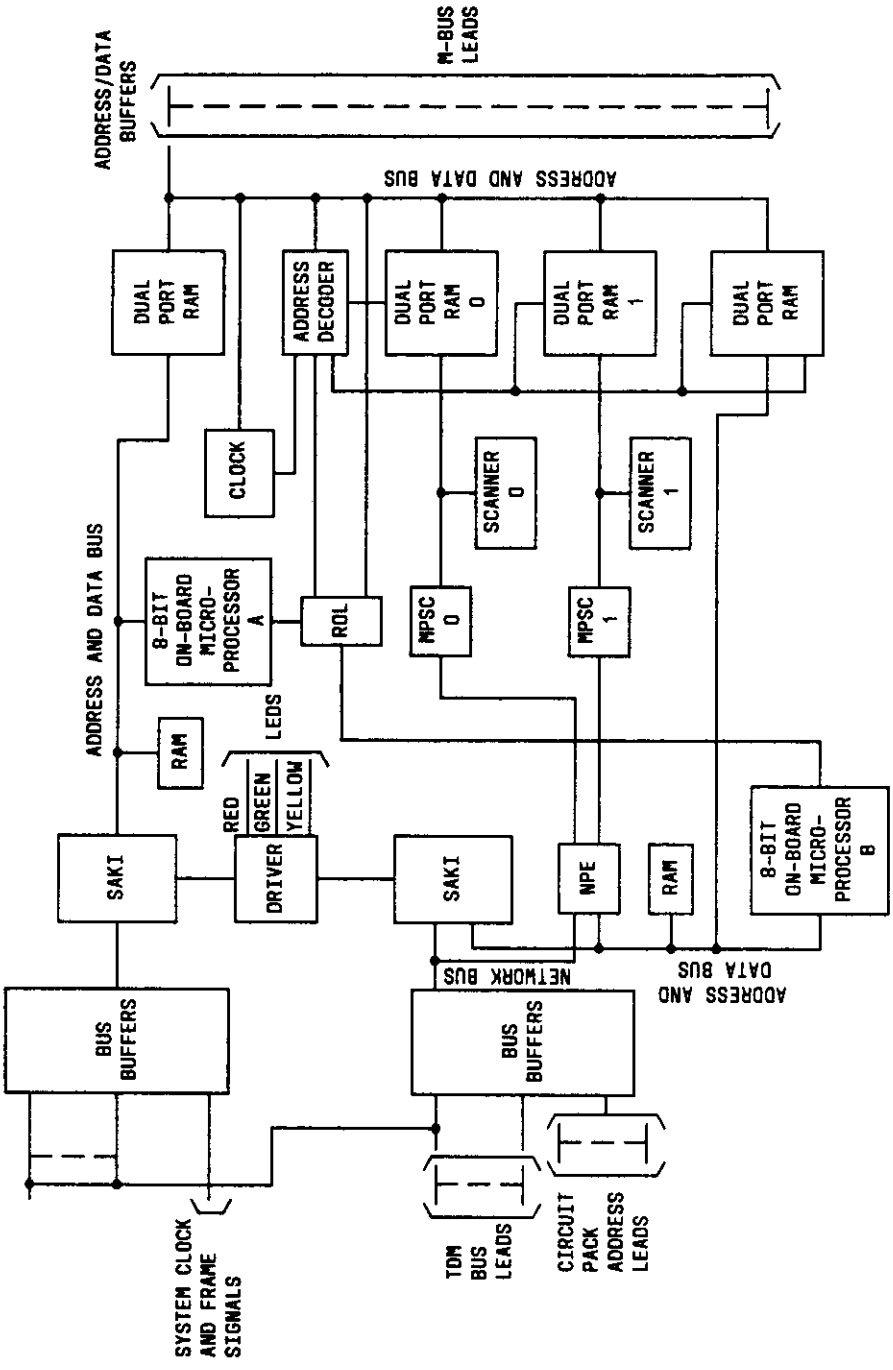

Figure 16. Network Control Circuit

8-Bit On-Board Microprocessor A With External RAM

The 8-bit on-board microprocessor A acts as a switch passing messages back and forth between the SPE and the on-board microprocessors located in the port circuits. It is the focal point for all uplink messages from the port circuits as well as the central distribution point for all downlink control messages. It continuously scans, over the TDM bus, the port circuit microprocessors for sanity and activity.

The 8-bit on-board microprocessor A also keeps track of the status of the three system clocks on both a combined and individual basis. As part of the restart sequence, the microprocessor must clear the clock after an interrupt and after a clock failure is detected. The external RAM stores control channel information and port related information.

The network interface circuitry for the 8-bit on-board microprocessor A consists of bus buffers and a SAKI. The bus buffers provide the interface between the TDM bus and the on-board data buses to the SAKI. The SAKI receives and transmits control messages on the first five time slots on the TDM bus A. It also controls the LEDs on the front of the circuit pack through a driver circuit. The 8-bit on-board microprocessor A communicates with the SAKI and external RAM over an address and data bus.

8-Bit On-Board Microprocessor B With External RAM

The 8-bit on-board microprocessor B provides the intelligence to communicate control information back and forth to the SPE through the 8-bit on-board microprocessor A. This microprocessor differs from the port circuit microprocessors in that it also has access to the SPE through a dual port RAM. This enables a distinct control driver to respond to call processing messages and to control the four DCP data channels provided by the scanner circuits.

The 8-bit on-board microprocessor B processes maintenance messages, network updates, downlink acknowledgments, and uplink requests received from the 8-bit on-board microprocessor A. All other messages are passed directly to and from the SPE through the dual-port RAM. The external RAM stores control channel information and port-related information.

The network interface circuitry for the 8-bit on-board microprocessor B consists of bus buffers, an NPE, and a SAKI. The bus buffers interface the TDM bus and the on-board data buses to the SAKI and the NPE.

The NPE serves as a switching network for the four DCP data channels provided by the scanner circuits by picking digital data from the correct time slot. It receives and transmits data to and from the scanner circuits. The network side of the NPE receives and transmits these data signals in parallel on the TDM bus. NPE operation is controlled by the 8-bit on-board microprocessor B over the address and data bus.

The SAKI transmits and receives control messages to and from the TDM bus. It is controlled by the on-board 8-bit microprocessor B in the same manner as the NPE. Under certain circumstances, such as the absence of polling by the SPE or detection of unexpected signals on the control time slots, it can reset the on-board 8-bit microprocessor B. When the SAKI receives a control message, it interrupts the on-board 8-bit microprocessor B to read the existing message before a new one arrives.

Scanner Circuits

The Network Control circuit pack contains two identical scanner circuits. It consists of a multi-programmable serial controller (MPSC) and a scanner. The MPSC is a sophisticated USART device that provides high level support for the scanner. The scanner transfers information between the MPSC (receiving data from the NPE serial channels) and dual-port RAMs (receiving data from the SPE) based on MPSC status and dual-port RAM pointers. Each scanner services two channels per MPSC with one dual-port RAM split between two channels.

The scanner processes data, EIA, and handshake packets and moves the contents to the proper location in the buffer shared with the SPE. For transmitting, the scanner performs baud rate emulation as it builds packets with data downloaded from the SPE.

Clock Circuit

The clock circuit consists of a timer, a battery, and an inverter. The timer is a single-chip, time-of-day clock. It indicates to the SPE the current time, day, and month. The lithium battery is a 3-volt supply used to back up the timer if system power is lost for extended periods of time. The inverter circuit properly operates the timer during battery backup.

M Bus Interface Circuit

The M bus interface circuit provides a communication interface with the SPE for the 8-bit on-board microprocessors A and B and the scanner processors. It consists of an address decoder circuit, a readable output latch (ROL) circuit, four dual-port RAMS and address/data buffers.

The address decoder circuit decodes address information that appears on the M bus with command signals. These command signals access the real-time clock, reset the 8-bit on-board microprocessor A and data channels, and operate the ROL circuit.

The ROL circuit is a control register and is readable and writable from the M bus. The ROL circuit allows the SPE to control the 8-bit on-board microprocessors A and B and provides an indication of clock failure.

The four dual-port RAMs provide the proper interface for each of the individual processors. The two dual port RAMs that interface the scanners to the SPE are identical. Each dual port RAM stores 512 eight-bit bytes.

The address/data buffers interface the Network Control circuit pack with the M bus address and data lines. The address lines from the M bus can drive up to two on-board devices. Address lines that are needed by more than two devices are buffered. The 16-bit wide M bus interfaces 8-bit wide memory components on the Network Control circuit pack. The correct bus buffer is selected according to the state of inputs to the address decoder circuit and the dual-port RAMS.

Processor

The Processor circuit pack is the general purpose vehicle that supports the System 75 multi-user, multiprocessor environment. Each system contains one Processor circuit pack. Power for the circuit pack (+5 volts dc) is provided on the backplane.

The Processor circuit pack consists of the following (see Figure 17):

- Central processing unit (CPU) and support circuitry
- Memory management circuit
- On-board memory
- On-board peripherals
- Bus buffers

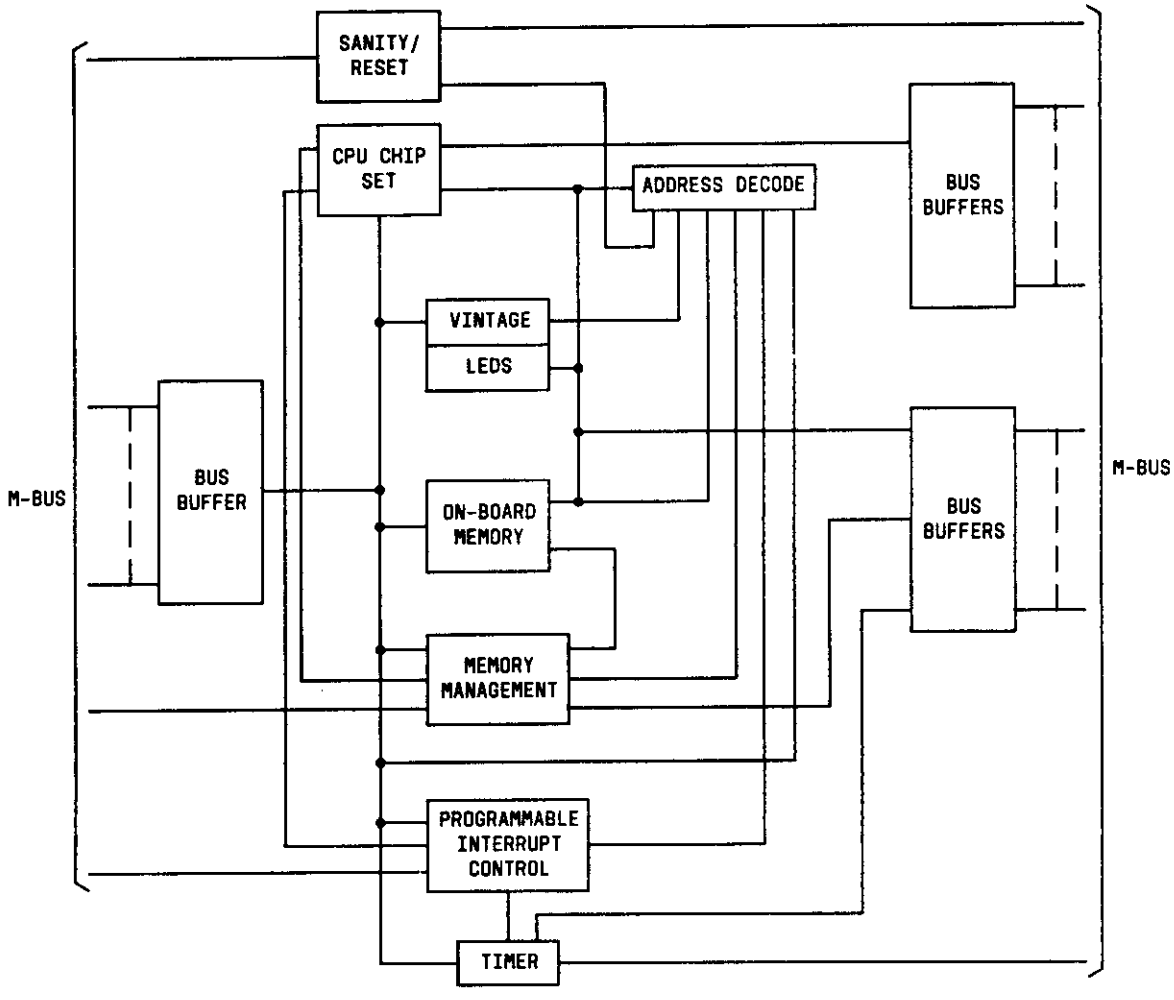

Figure 17. Processor Circuit

CPU and Support Circuitry: The CPU and support circuitry consist of the following:

- CPU Chip Set
- Sanity/Reset Circuit
- Address Decode Circuit

CPU Chip Set

The CPU chip set includes a 16-bit microprocessor and clock generation and bus control logic. The CPU executes stored programs to effect call processing or data processing functions. It provides the basic high-level control over the system.

Sanity/Reset Circuit

The sanity/reset circuit provides system reset functions. Sanity control is provided by a watchdog timer circuit that is triggered periodically by the CPU. A reset stimulus can originate from a power up of the Processor circuit pack, the Maintenance circuit pack, the Network Control circuit pack, or a CPU sanity timeout.

Address Decode Circuit

Each on-board peripheral is assigned a unique address in I/O space to allow independent CPU control. In addition, each set of on-board memory devices is assigned a range of memory space addresses. The decoding circuitry translates on-board addresses into individual device select signals.

Memory Management Circuitry: The memory management circuitry supports a high level multiprocess software environment. The bootstrap program in erasable programmable read-only memory (EPROM) sets up an initial environment and enables the memory management circuitry. The memory management circuitry consists of the following:

- Segment descriptor RAM
- Memory management control circuit
- Address arithmetic and logic unit (ALU)
- Address comparator
- Exception logic circuit

A set of 16 segment descriptors contained in RAM controls access to all of main memory (Memory circuit pack) on the M bus. The memory management control circuit provides the status of the memory management circuit to the CPU and allows the memory management circuit to be enabled by bootstrap or diagnostic programs.

The virtual addresses produced by the CPU are translated into a physical M bus address by the ALU. The address comparator checks that the virtual addresses are valid.

The exception logic circuit detects memory management circuit commands that cannot be executed and certain hardware faults. It logically combines the exceptions and faults to create a non-maskable interrupt (NMI) to the CPU. The cause of the NMI is latched and made available to the CPU to allow recovery from the fault.

On-Board Memory: The on-board memory consists of read-only memory (ROM) and RAM. This memory does not store any applications related software. The ROM contains the bootstrap and low-level diagnostic programs.

On-board Peripherals: The Processor circuit pack on-board peripherals consist of the following:

- Vintage straps and LEDs
- Programmable interrupt controller (PIC)
- Timer

Vintage Straps and LEDs

Four vintage straps identify circuit pack hardware vintage to the CPU. The three LEDs indicate CPU status—red (failure), green (test), and yellow (busy).

PIC

The PIC logically combines the eight sources of maskable interrupt to a single interrupt to the CPU. In addition, the PIC provides priority arbitration and masks each source independently. Four of the interrupts are from off-board sources and four are from the on-board timer.

Timer

The timer provides five programmable timer channels. Four of the channels are connected as maskable interrupts to the PIC. The fifth output is connected to the M bus for S bus access.

Bus Buffers: The bus buffers interface all data, address, and command lines to the M bus. Some CPU status signals are also buffered. This isolates the circuit pack from the M bus and allows for other access to the M bus.

Memory

The Memory circuit pack provides a medium for storage and execution of the software associated with system operation. This software includes the operating system, call processing, system data, system translations, and other related programs.

Each system contains one Memory circuit pack. Power for the circuit pack (+5 volts dc) is provided on the backplane.

The Memory circuit pack (See Figure 18) consists of the following:

- Address and data buffers
- Board and I/O select logic circuit
- Memory array
- Memory select and driver
- Error detection and correction logic circuit
- Timing and control logic circuit
- Maintenance logic

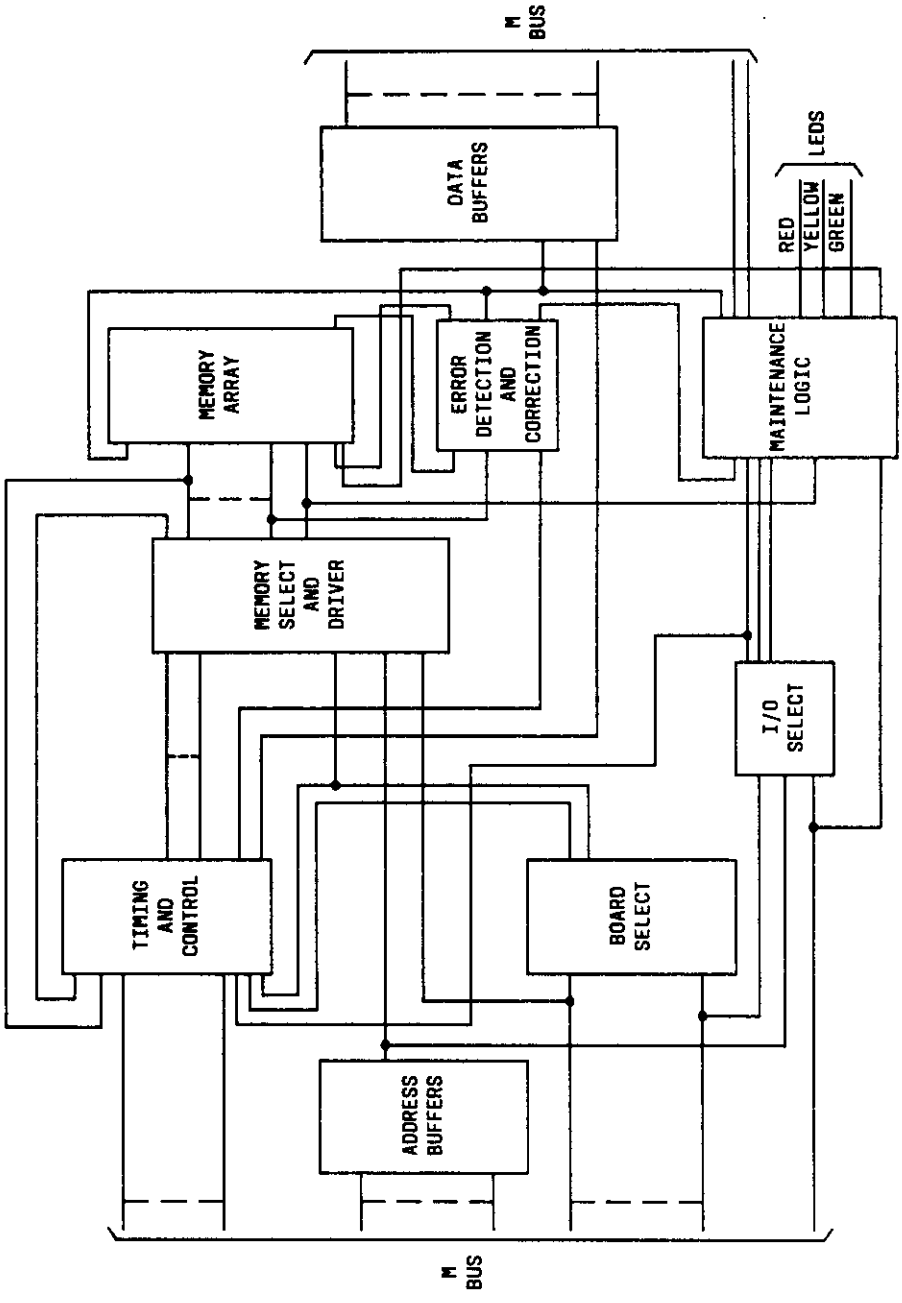

Figure 18. Memory Circuit

Address and Data Buffers: The address and data buffers interface the Memory circuit pack to the address and data lines on the M bus.

Board and I/O Select Logic Circuit: The board and I/0 select logic circuit prevents improper accessing of the Memory circuit pack. It uses the upper seven address lines and the four memory identification and processor identification address lines on the M bus.

Memory Array: The memory array consists of eighty-eight 256K dynamic RAM devices. These devices are configured in an arrangement of four 22-bit wide banks. Valid memory data is 16 bits wide. The remaining 6 bits are dedicated to check bit storage.

Memory Select and Driver: The memory select and driver selects and drives the appropriate bank of RAM in the memory array. It can force a refresh during heavy access times, determine which bank of RAM has been selected, and multiplex the memory array addresses.

Error Detection and Correction Logic Circuit: The error detection and correction logic circuit generates and latches check bits associated with each word during a memory write. These check bits are also used to check data on memory reads. The error detection and correction logic performs single bit correction and multiple bit correction.

Timing and Control Logic Circuit: The timing and control logic circuit establishes the basic memory refresh rate, memory cycle time, and error detection and correction timing. It also arbitrates conflicting memory cycles (refresh requests, M bus requests, and S bus requests). Design of the timing and control logic circuit allows two modes of memory access, traditional request and advanced start request.

A traditional request is started by memory commands from the processor or peripheral processor via the board select logic circuit. This type of memory access allows the local processor or peripheral processor to access the Memory circuit pack when there is an active refresh cycle taking place at the time of the request.

An advanced start request is started by an address latch strobe. This type of memory access allows for shorter memory access time. This is accomplished by presetting the request logic circuit and performing arbitration functions in advance of the actual memory access.

Maintenance Logic Circuit: The maintenance logic circuit provides several programmable optional modes of operation. These modes allow for testing and continued operation during certain failure conditions. The maintenance logic circuit also controls the three LEDs on the front of the circuit pack—red (failure), green (test), and yellow (busy).

Tape Control

The Tape Control circuit pack interfaces the high capacity minirecorder (HCMR) to the M bus. The interface provides control and data transfer between the M bus and the HCMR. The Tape Control circuit pack (see Figure 19) consists of the following:

- Decode and control circuit
- Data transceivers
- Address buffers
- Vintage and code circuit
- Termination circuit

The decode and control circuit is a logic array that maps address and command signals on the M bus into device select and timing signals required to interface the HCMR. The data transceivers provide a bidirectional transmission path between the M bus and the HCMR. The address buffers buffer the address lines from the M bus to the HCMR and use the decode and control circuit to generate a translation of interface commands for the HCMR. The vintage and code circuit indicates circuit pack vintage to the SPE and provides circuit pack status on the faceplate LEDs—red (failure), green (test), and yellow (circuit busy). The termination circuit includes a current programming resistor that controls the current limit on the circuit pack and provides terminations for unused HCMR signals.

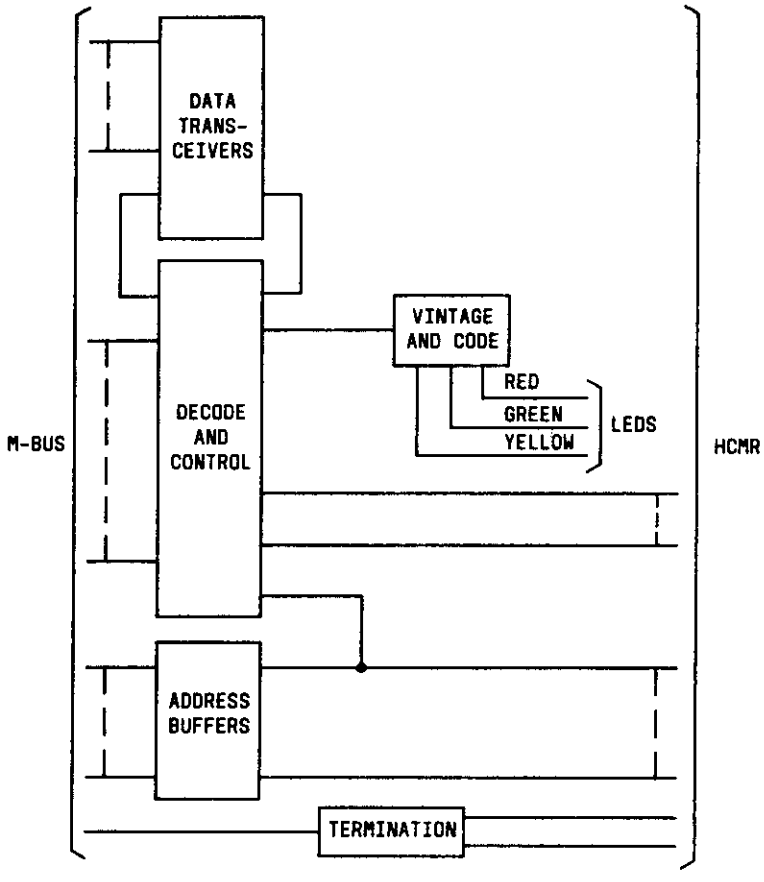

Figure 19. Tape Control Circuit

HIGH CAPACITY MINIRECORDER

General

The high capacity minirecorder (HCMR) provides a nonvolatile system bootstrap and translation storage device. The HCMR uses the incremental operating mode. In the incremental mode, data is efficiently read or written one single block of data at a time. The HCMR tape cartridge stores up to 12M bytes of data in the incremental mode.

Tape Cartridge

Data is written sequentially, a block at a time, on each of the five tracks on the tape cartridge. The tracks are arranged in serpentine fashion. Subsequent access, for reading or editing, can be done randomly over the blocks previously written.

The high density digital tape in the cartridge is 600 feet (183 m) long. During read or write operations, the tape speed is 50 inches (127 cm) per second. During search operations, the tape speed is 100 inches (254 cm) per minute.

High Capacity Minirecorder Circuit Packs

The HCMR contains four circuit packs (see Figure 20) housed in an apparatus mounting located in the power distribution unit. The four circuit packs are as follows:

- Controller
- Data Electronics/Servo
- Transport
- Power Supply

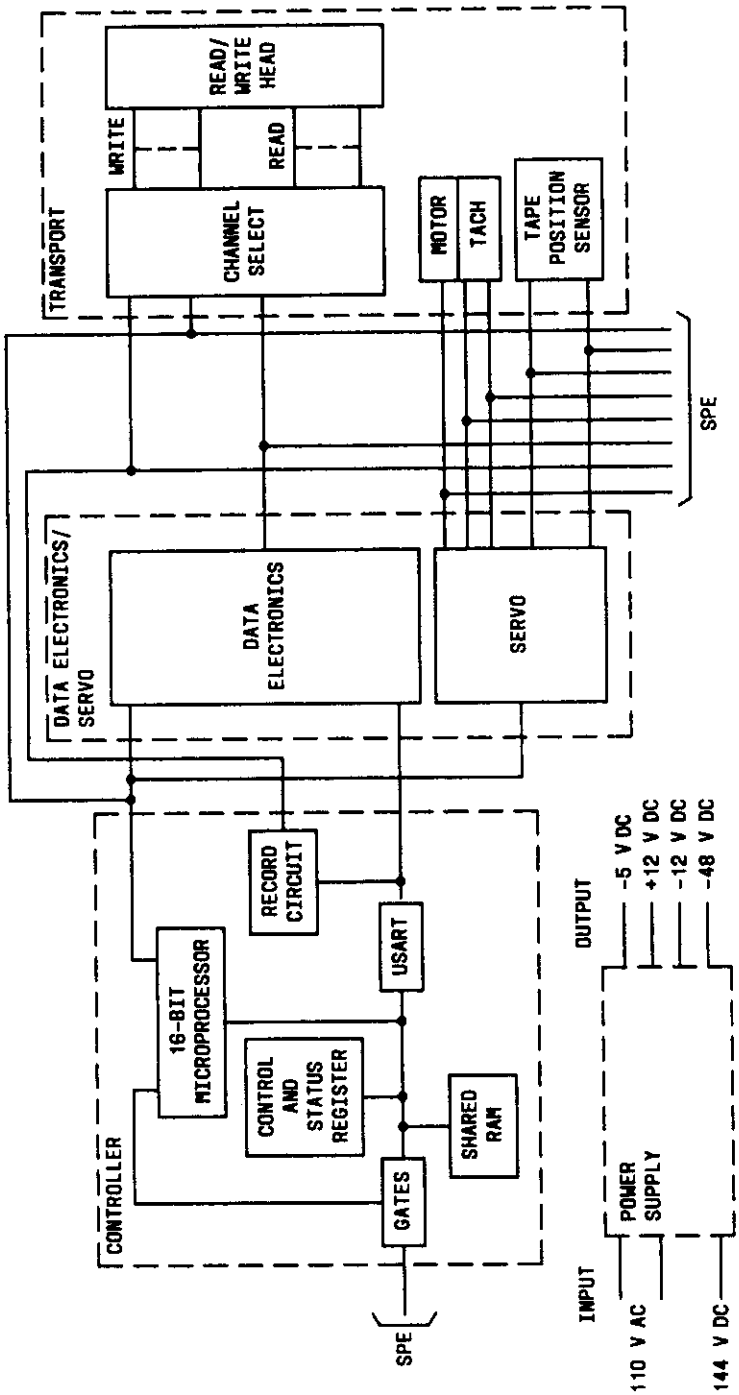

Figure 20. High Capacity Minirecorder Circuit

The circuit packs in the HCMR are interconnected by a bus on the backplane of the apparatus mounting. The Controller, Data Electronics/Servo, and Transport circuit packs have three LEDs on the faceplates—red (failure), green (test), and yellow (in-use). These three circuit packs also have an 8-bit vintage register that can be read by the Controller and reported to the SPE.

The Power Supply circuit pack has two green LEDs. When the upper LED is dark, input power is not present. When the lower LED is dark, output voltages are not within tolerances.

Controller

The Controller circuit pack main component is a 16-bit microprocessor. Programs executed by this microprocessor generate the data block format, select the tape direction and speed, control the read/write electronics, and monitor the other HCMR circuit packs.

The interface to the SPE via the Tape/Control circuit pack is via the shared RAM and the hardware command and status registers. The shared RAM buffers one block of data and passes commands and status between the Controller circuit pack and the SPE.

A high speed USART does the parallel-to-serial data conversion when writing on tape and the serial-to-parallel to serial conversion when reading from tape. This same USART also does a cyclic redundancy check (CRC) for each frame of data.

The record circuitry digitally encodes the output of the USART for transmission to the Transport circuit pack. The bit stream is precompensated for peak shift.

Data Electronics/Servo

The data electronics portion of this circuit pack performs the read function. It interfaces the single digital channel on the Controller circuit pack to the selected read head analog output in the Transport circuit pack.

The servo controls the dc motor on the Tape Transport circuit pack. Servo control logic is contained in an 8-bit microprocessor. The servo responds to one of five velocity commands from the Controller circuit pack—stop, normal speed forward or reverse, and search speed forward or reverse.

Tape Transport

The Tape Transport circuit pack contains the 5-track read/write head and a permanent magnet dc motor with tachometer. It also contains an optical sensor that responds to the punched holes in the tape to provide the basic information used by the Controller circuit pack to determine the beginning and end of tape, load point, and early warning positions. Mechanical sensors indicate when the cartridge is in place and show the write protect status.

Power Supply

The Power Supply circuit pack supplies the following voltages to the HCMR circuit packs.

Voltage	Tolerance
+5 volts dc	5%
+12 volts dc	5%
-12 volts dc	5%
-48 volts dc	13%

Input power is 110 volts ac or 140 volts dc for battery backup.

APPLICATIONS PROCESSOR INTERFACE

The interface to an Applications Processor/Adjunct (AP) is provided by the following three circuit packs:

- Interface 1
- Interface 2
- Interface 3

As shown in Figure 1, these circuit packs are connected to the M bus. Interface 1 and Interface 2 are connected by the S bus. The S bus contains 16 data, 24 address, 5 parity, 10 interrupt, and 11 control lines. The S bus is located on the backplane of the control carrier and provides the medium for the SPE to transfer data to or from the AP.

Interface 1

The Interface 1 circuit pack serves as a gateway between the SPE's local M bus and the S bus by performing the decoding and arbitration necessary to allow communication with the Interface 2 circuit pack. When the SPE indicates that it wishes to perform an operation, the Interface 1 circuit pack secures the M bus for the SPE to lock out Interface 2 from the local M bus. The SPE then puts the address of the location it wishes to access onto the M bus.

The Interface 1 circuit then determines if this a local address or that of Interface 2 (remote address). If it is a local address, the cycle continues in a normal manner with the Interface 1 remaining in an unchanged state for the duration of the process. If it is a remote address, the Interface 1 circuit allows the SPE to gain access to the S bus. The process is reversed if Interface 2 is attempting to access the SPE. When this happens, the Interface 1 circuit blocks the SPE from its own M bus, allowing Interface 2 clear access to it.

The Interface 1 circuit pack consists of the following circuitry (see Figure 21):

- S bus decoder and arbitration circuitry
- M bus decoder and arbitration circuitry
- Control circuit
- XACK/Clock fail circuit
- Bus buffers
- Parity circuit
- Spend circuit
- I/O bus circuit

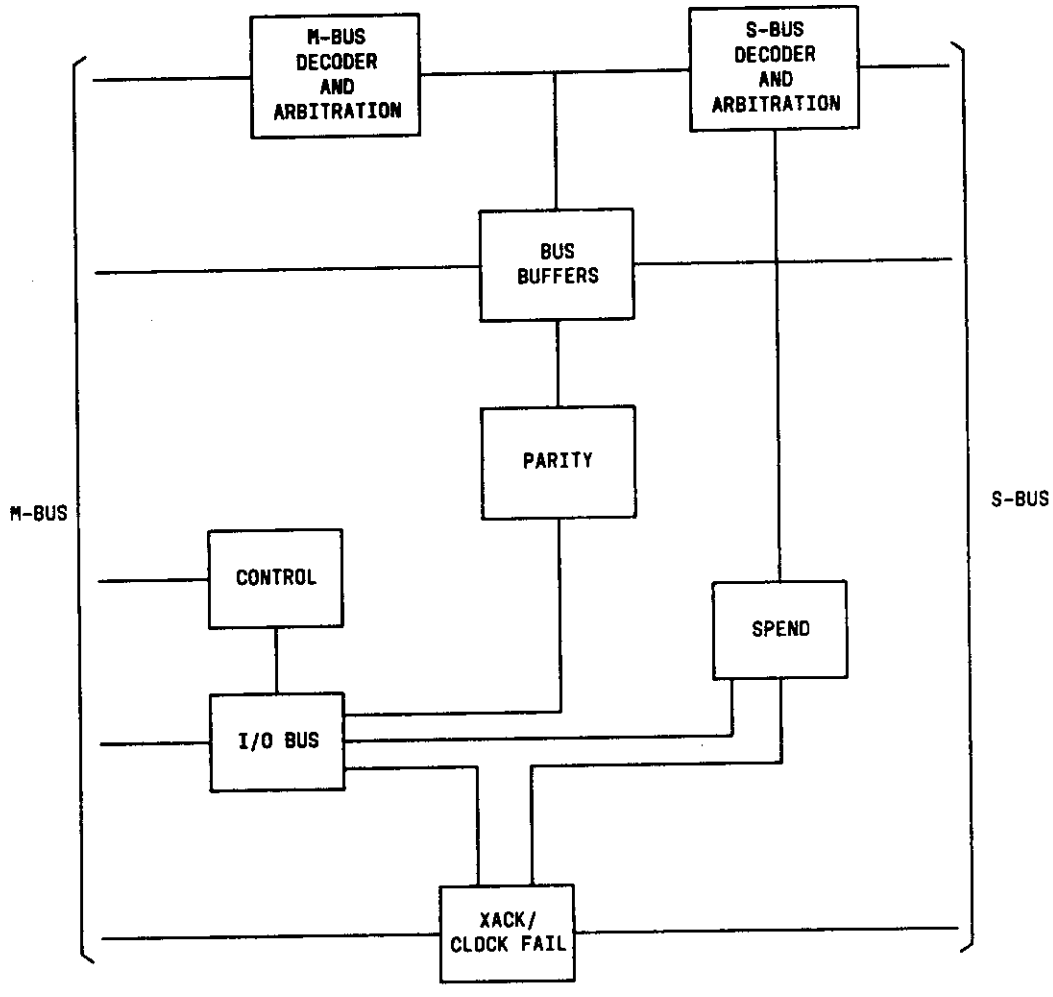

Figure 21. Interface 1 Circuit

S Bus Decoder and Arbitration Circuit

The S bus arbitration circuit determines whether Interface 2 or the SPE will actually be allowed to gain control of the S bus. The decoder monitors the S bus address, data, and command leads to determine when the Interface 1 circuit is addressed. The decoder also determines whether the SPE or the Interface 2 requesting the S bus has the highest priority.

M Bus Decoder and Arbitration Circuit

The M bus arbitration circuit determines whether a local command or an S bus cycle accessing the local memory has priority. The decoder circuit is a 32-bit input decoder that determines when the Interface 1 circuit is being addressed on the M bus.

Control Circuit

The control circuit provides internal board signals that are used to control the various functions performed by the Interface 1 circuit pack.

XACK/Clock Fail Circuit

The transfer acknowledge (XACK) circuit tells the SPE or the Interface 2 when to terminate a cycle. The clock fail circuit checks for the presence of the S bus clock signal.

Bus Buffers

The bidirectional bus buffers connect all address, data, and command lines to both the M bus and the S bus. The direction of these buffers is determined by whether or not the SPE is acting as a source or destination for the transfer being performed.

Parity Circuit

Even parity is used on both the address and data bus. This circuit checks the signals at the M bus destination after they are sent across the S bus by the Interface 2 or the SPE. The parity bits never appear on the M bus.

Spend Circuit

The spend circuit is a 16 microsecond timer that causes a timeout to occur if the SPE does not get the S bus within 16 microseconds of request. Once the S bus is obtained, the spend timer is reset.

I/O Bus Circuit

The I/O bus circuit interfaces the Interface 1 I/O (ID, vintage, and NMI registers) to the SPE's M bus.

Interface 2

The Interface 2 circuit pack handles message traffic between the SPE and the AP. Its other functions include handling BX.25 protocol and supporting Call Detail Recording and Reporting (CDRR), Leave Word Calling, and Message Center. The Interface 2 circuit pack communicates with the SPE by means of the S bus and the Interface 3 circuit pack by means of the M bus.

The Interface 2 circuit pack consists of the following circuitry (see Figure 22):

- Processor and timing circuit
- M bus buffers
- Decoders/ACYL circuit
- Local Cycle Arbitrator
- I/O Ports
- DRAM control circuit
- DRAM
- Memory buffers and ROM
- NMI and LEDs
- XACK/WAIT state circuit
- Parity circuit
- S bus interface (locks/gates/enable) circuit
- S bus arbitrator
- S bus interface (interrupt queue)
- P/O S bus interface buffers
- S bus interface buffers

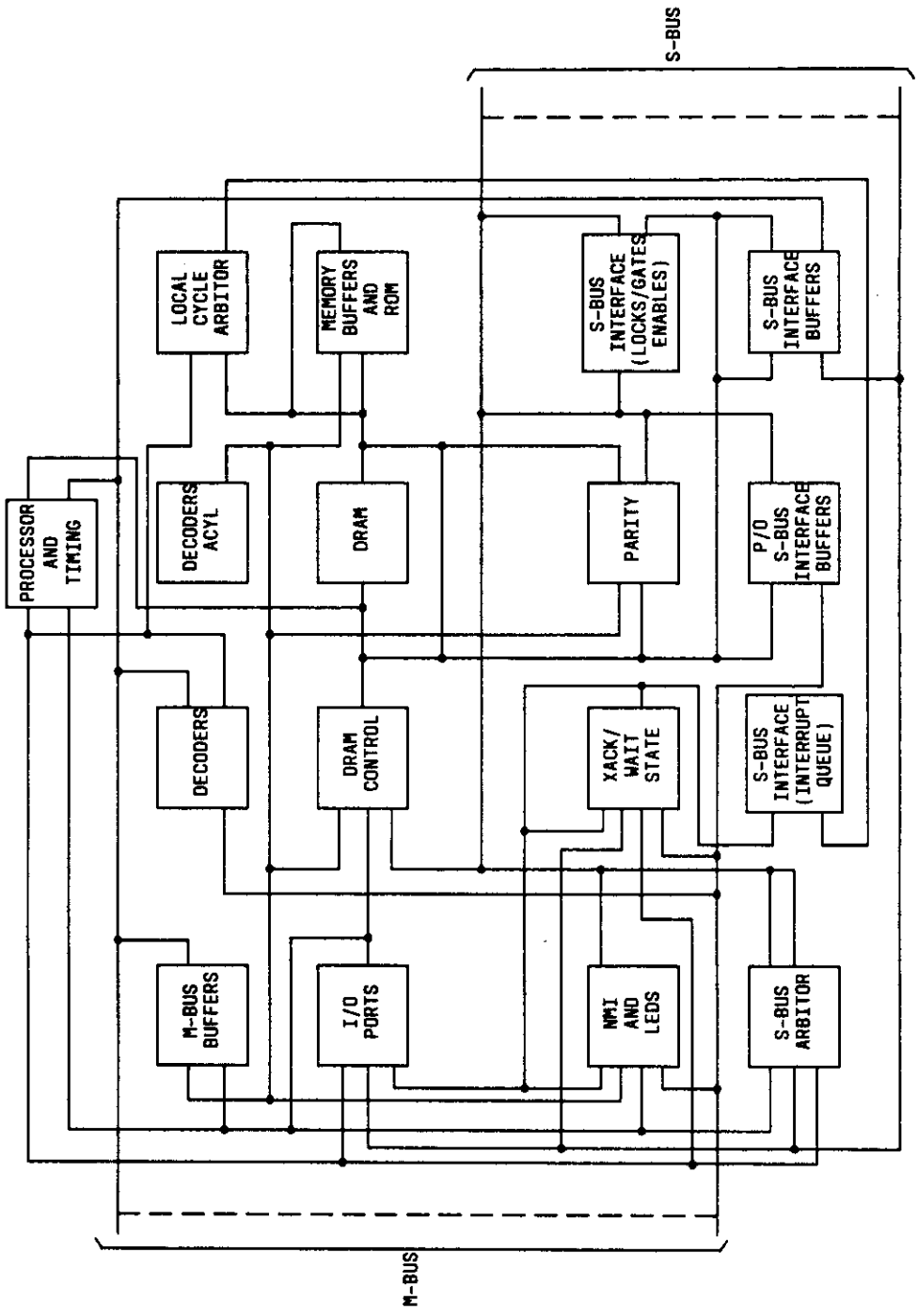

Figure 22. Interface 2 Circuit

Processor and Timing Circuit

The processor and timing control circuit provides all timing and control signals necessary to provide basic functions for the entire circuit pack. It decodes basic board transactions, initiates board reset, provides address and data decoding, and controls circuit pack sanity.

M Bus Buffers

These buffers interface the processor circuit to the M bus. They receive or transmit address and control information between the Interface 2 circuit pack and any other circuit packs connected to the M bus.

Decoders

The decoders detect processor ID's and certain S bus address bits to determine interrupts and remote addresses. They also handle decoding that determine whether S bus gates are locked or unlocked and the on/off cycle of the red LED on the front of the circuit pack.

Decoders/ACYL Circuit

This set of decoders handles decoding for commands, on-board timers, and non-maskable interrupts (NMIs). They decode on-board operations such as memory or programmable read-only memory (PROM) chip selects and determine whether an operation is on board or off board.

Local Cycle Arbitor

This arbitor controls whether the Interface 2 circuit pack or a remote processor has access to the Interface 2 circuit pack's local memory.

I/O Ports

The I/O ports connect the local peripherals on the Interface 2 circuit pack.

DRAM Control Circuit

This circuit provides all timing and control functions for the on-board 128 kb dynamic RAM (DRAM) circuit.

DRAM

This is the 128 kb local DRAM.

Memory Buffers and ROM

The ROM can only be accessed by the Interface 2 circuit pack and is used after reset to initialize the board, run diagnostics, and provide a monitor.

NMI and LEDs

The Interface 2 circuit pack supports 12 non-maskable interrupts (NMIs) and 8 maskable interrupts. An eight bit read/write I/O port controls the LEDs on the front of the circuit pack and the sanity timer mask.

XACK/WAIT State

This circuit monitors every bus cycle and sends a transfer acknowledge signal to a source processor indicating the requested transfer has been completed. Depending on the activity, a timeout may occur or wait states are inserted.

S Bus Interface (Locks/Gates/Enables)

This is the Interface 2 circuit pack S bus control section. It determines if the Interface 2 circuit pack's access to the S bus is locked or unlocked.

S Bus Arbitor Circuit

This circuit determines whether the SPE or the Interface 2 requesting the S bus will actually be allowed to gain control of the bus and use it. This is determined on a first come, first served basis.

S Bus Interface (Interrupt Queue)

This circuit stores the ID of the SPE that sent a message to Interface 2. The IDs are stored here until the Interface 2 circuit pack services the queue.

P/O Bus Interface Buffers

This set of buffers are used to interface command and parity check bits to the S bus.

S Bus Interface Buffers

These bidirectional buffers connect all address and data lines to both the M bus and S bus. The direction of these buffers is determined by whether or not Interface 2 is acting as a source or destination for the particular transfer being performed.

Interface 3

The Interface 3 circuit pack provides a link between the TDM bus and the Interface 2 circuit pack. Circuits on the Interface 3 circuit pack terminate the DCP and provide some link level support for the Interface 2 circuit pack. The Interface 3 circuit pack contains four separate ports.

The Interface 3 circuit pack consists of the following circuitry (see Figure 23):

- Common circuitry
  - Bus buffers
  - SAKI
  - NPE
  - On-board microprocessor with external RAM
- M bus interface circuit
- Traffic controller circuits and dual-port RAM
- DUCK-TRIC-Microcomputers

Common Circuitry

The Interface 3 common circuitry provides the same general function as the intelligent port common circuitry.

M Bus Interface Circuit

This circuit provides address decoding and chip select logic as well as a transfer acknowledge (XACK) signal during memory and I/O accesses from the M bus. Also included in this circuit is the interrupt latch and interrupt line drivers. The interrupt latch guarantees sufficient hold time for the programmable interrupt controller in the Interface 2 circuit pack.

Traffic Controller and Dual-Port RAM Circuits

The two traffic controllers provide the data terminal equipment (DTE) portion of the EIA interface. The dual-port RAMs provide shared memory interface to the Interface 2 circuit pack.

DUCK-TRIC-Microcomputers

There are four identical DUCK-TRIC-Microcomputer circuits on the Interface 3 circuit pack. The microcomputer handles the control portion of the DCP link. Under firmware control, the microcomputer handles EIA updates and DCP handshaking. The DUCK generates and interprets DCP clock update messages, and provides the client interface portion of the data module. The TRIC multiplexes the data stream from the DUCK and the control stream from the microcomputer and provides an interface to the network for the data module.

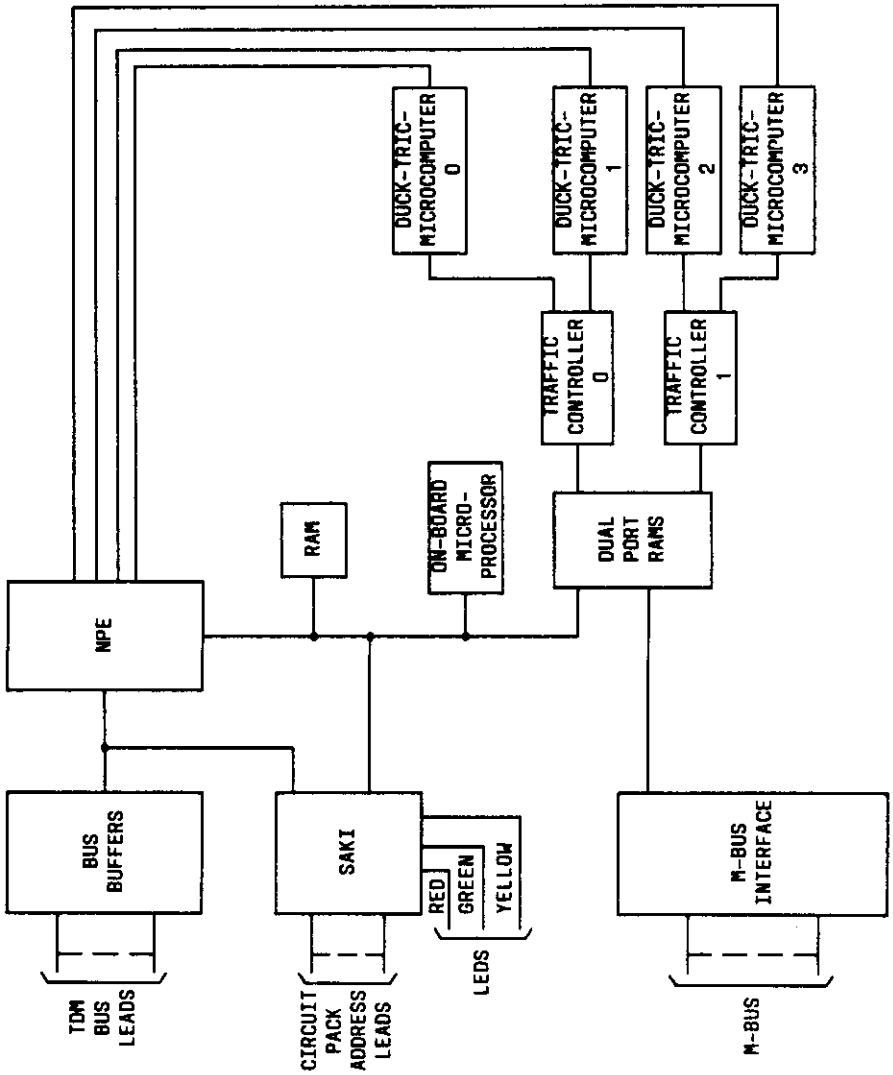

Figure 23. Interface 3 Circuit

MAINTENANCE CIRCUIT

General

The Maintenance circuit pack is a peripheral processor for the SPE. The Maintenance circuit pack communicates with the SPE on the M bus via dual port RAM and I/O registers. The I/O registers are accessed by the SPE using I/O read and write for high speed polling and backup communications. Two dedicated leads between the Maintenance circuit pack and the SPE provide signaling for the GO-TO-SLEEP command that disables the SPE. The leads also allow the Maintenance circuit pack to monitor SPE sanity.

The Maintenance circuit pack functions as follows:

- Originates alarms to the Initialization and Administration System (INADS) via a trunk circuit located on the circuit pack
- Includes a digital modem for reliable synchronous communication with INADS
- Provides alarm LEDs for system status
- Provides emergency transfer switch and emergency transfer control
- Monitors and controls the reset condition and sanity of the SPE
- Monitors and controls the power units and battery charger
- Monitors the cabinet environment
- Provides maintenance circuit pack diagnostics
- Provides direct access to dedicated system administration terminal (SAT)

When the Maintenance circuit pack is initialized, the SPE sends the Maintenance circuit pack necessary administration data (INADS phone number, product identification, and software vintage).

SPE Monitoring and GO-TO-SLEEP Control

The SPE is automatically reset every time a sanity time-out occurs. The SPE controls the recovery after a reset. The Maintenance circuit pack monitors the SPE sanity timer and, if the rate of sanity time-outs are excessive, the SPE is shutdown via the GO-TO-SLEEP signal. This signal becomes active after the threshold has been reached. When the threshold is reached, the Maintenance circuit pack will do the following:

- Put the SPE to sleep
- Invoke emergency transfer
- Notify INADS
- Update alarm LED status

After 20 minutes, the SPE is awakened. If no sanity timeouts occur in the SPE within 15 minutes, the system is taken out of emergency transfer and returned to SPE control. If a time-out does occur within 15 minutes, the SPE is put to sleep again for 1 hour. If the SPE does not have a sanity time-out within 15 minutes after being awakened, emergency transfer is disabled and the SPE regains control of the system. If a time-out occurs within this 15 minute period, the SPE is put to sleep again. This process is repeated until the SPE becomes sane.

System Interactions

The actions by the Maintenance circuit pack for a given situation depend on the state of the SPE sanity. The following examples explain how the Maintenance circuit pack interacts with the system. Case 1 shows that the SPE is operating properly (has not been put to sleep). Case 2 shows that the SPE has been put to sleep.

Alarm Origination

For case 1, the following steps apply:

1. The SPE sends a message to the Maintenance circuit pack.
2. The Maintenance circuit pack attempts to call INADS and reports back to the SPE on the success or failure of the call.
3. When the connection to INADS is complete, the data from the SPE is transmitted.

For case 2, the following step applies:

1. The Maintenance circuit pack calls INADS to report the system status (SPE-DOWN MODE).

Alarm LED Status Update

The alarm LEDs on the Maintenance circuit pack (see Table B) are updated as follows in a case 1 situation:

1. The SPE sends an update message to the Maintenance circuit pack.
2. The Maintenance circuit pack updates its LED status.

For a case 2 situation, the Maintenance circuit pack updates the appropriate LED as alarms are detected.

TABLE B. Maintenance Circuit Pack Leds

LED	Color	Lighted Indication
ALM	Red	A failure has been detected on the Maintenance circuit pack.
TST	Green	The system is running a set of tests on the Maintenance circuit pack.
BY	Yellow	Carrier detect is present on SAT.
MJ	Red	Major failures causing critical degradation of service have been detected.
MN	Red	Failures causing marginal degradation of service have been detected.
WRNG	Yellow	Failures causing no noticeable degradation of service have been detected.
ENV	Green	Environmental problem such as high temperature has been detected.
EXF	Red	System is in emergency transfer.

System Administration Terminal Interface

When the maintenance port detects data terminal ready and case 1 applies, the Maintenanc circuit pack functions as follows:

1. Sends a wake-up message to the SPE and waits for the SPE to transmit data t the system administration terminal (SAT) via its dual-port RAM.
2. Remains in passive mode, passing data on a character-by-character basis (fo administration and maintenance forms) between the SPE and the SAT.

When case 2 applies, the Maintenance circuit pack functions as follows:

1. Informs INADS that the SPE has been put to sleep (SPE-DOWN MODE).

The INADS terminal user then interfaces with the command interpreter in the Maintenance circuit pack. The prompt is different from the prompt provided by the SPE.

Emergency Transfer Control

The emergency transfer control switch located on the Maintenance circuit pack faceplate has three positions: ON, AUTO (automatic), and OFF. When the switch is in the ON position, the system is forced into emergency transfer; the Maintenance circuit pack cannot change this state. The AUTO position gives the Maintenance circuit pack full control over emergency transfer. When the switch is in the OFF position, the Maintenance circuit pack cannot invoke emergency transfer. The Maintenance circuit pack informs the SPE when the emergency transfer switch position changes.

Maintenance Circuit Pack

The Maintenance circuit pack (see Figure 24) consists of the following:

- 8-bit on-board microprocessor
- Chip select decoder
- Timer and interrupt controller
- Three I/O ports
- LED drivers
- Dual-port RAM
- Decoder
- Two Multi-Programmable Serial Controllers (MPSCs)
- RAM and ROM
- Digital Modem Circuit
- CO trunk circuit
- Voltage converter
- Clock timer

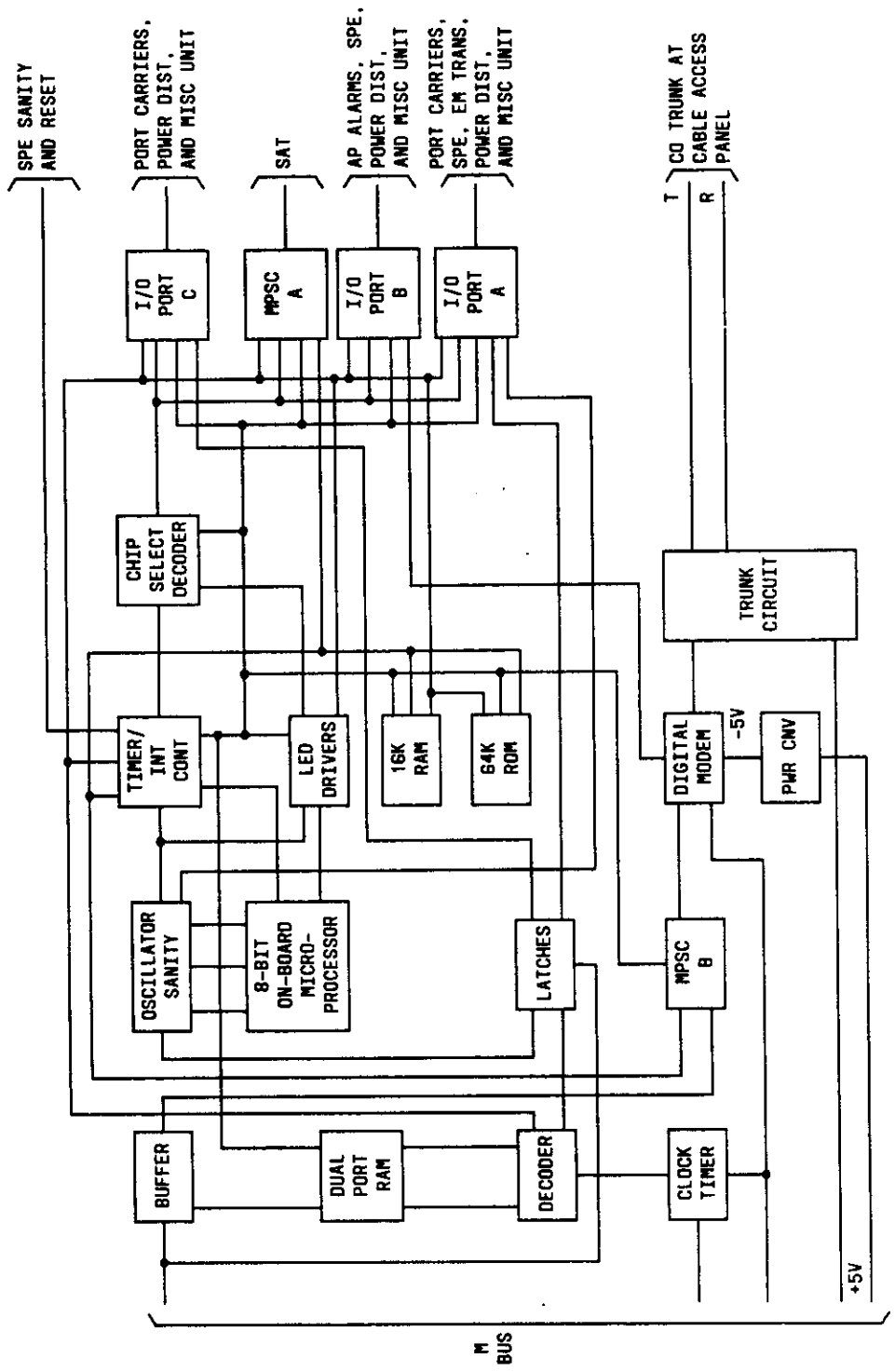

Figure 24. Maintenance Circuit

On-Board Microprocessor: The microprocessor controls the Maintenance circuit pack. The associated oscillator and sanity circuit controls the timing and ready lines to the microprocessor and keeps the microprocessor sane.

Chip Select Decoder: This circuit selects one of 20 devices to interact with the microprocessor. These devices include the on-board RAM and ROM and off-board devices via the port I/O circuits and MPSC A.

Timer and Interrupt Controller: The timer generates the three clock signals used on the Maintenance circuit pack.

- SAT baud rate
- CO trunk circuit clock rate
- Basic interrupt timing signal for the microprocessor

These signals are all software programmable. The interrupt controller provides the only means for the SPE to interrupt the on-board microprocessor.

I/O Ports: The three I/O port circuits interface the Maintenance circuit pack and peripheral devices. I/O port circuit A makes the SPE capable of taking the on-board microprocessor out of a reset condition. It controls all LEDs on the front of the circuit pack except for the in-use LED. It also provides guarded output control of the following:

- Emergency transfer relay
- Battery disconnect
- SPE GO-TO-SLEEP command
- Port Carrier power units

I/O port circuit B monitors the AP alarms. It also monitors on-board circuitry for the SPE, emergency transfer condition, setting of the emergency transfer switch of the front of the circuit pack, ac input, and battery charge rate. It controls the following:

- Resets of MPSC A and B and the digital modem
- Transmit and receive gain of the trunk circuit codec
- Guard circuit for I/O port A

I/O port circuit C reads the data written by the SPE to the Maintenance circuit pack. It monitors the reset condition of the on-board microprocessor during power up, minor and major environmental alarms, and power units in the port carriers and control carriers. It controls the following:

- Overcharge LED on the power distribution and miscellaneous unit
- In-use LED on the front of the circuit pack
- Reset condition of the I/O register that is written to by the SPE
- Trunk circuit dial outpulsing relay and hybrid balance

LED Drivers: This circuit provides the interface to the LEDs on the front of the circuit pack that are controlled by the port I/O circuits.

Dual-Port RAM: The dual-port RAM provides a communication path between the Maintenance circuit pack and the SPE. Data from the Maintenance circuit pack destined for the SPE is written into the dual-port RAM. The dual-port RAM, along with the decoder, place the data on the M bus data lines.

Decoder: The decoder allows the Maintenance circuit pack to recognize information received from the SPE. The decoder starts a timer in the SPE that signals the SPE when to resume operation.

MPSCs: Two MPSCs (A and B) are located on the Maintenance circuit pack. MPSC A provides two asynchronous channels to the Maintenance circuit pack. These channels are connected to EIA connectors on the rear of the control carrier (TERM and DTE). The SAT uses the TERM connector; the DTE connector is for future use. MPSC B provides a synchronous and asynchronous channel for the digital modem.

RAM and ROM: The Maintenance circuit pack 16K RAM and 64K ROM are used by the on-board microprocessor.

Digital Modem Circuit: The digital modem circuit consists of a USART, a microprocessor, a digital signal processor (DSP), and a shift register. It interfaces the analog trunk circuit to the digital part of the Maintenance circuit pack.

CO Trunk Circuit: The CO trunk circuit consists of a hybrid and a codec. It takes the data from the digital modem, converts it to analog, processes it, and supplies it to tip or ring of a trunk circuit.

Voltage Converter: This circuit converts the +5 volts dc on the backplane to the -5 volts dc required by the digital modem.

Clock Timer: This circuit uses the 2.048-MHz, 160-kHz, and 8-kHz input signals to generate the sync pulses necessary for the digital modem DSP and the trunk circuit codec.

Figures 25 and 26 show the power distribution schemes for the 2-carrier and 5-carrier System 75 cabinets, respectively. Five-conductor power distribution cables connect the power distribution unit to the power units in the carrier, to the HCMR, and to the 397A battery charger.

The power distribution cables provide 115-volt ac power on three of the leads during normal operation and 144-volt dc power on the other two leads during emergency transfer. The 144-volt dc power is not provided for the battery charger.

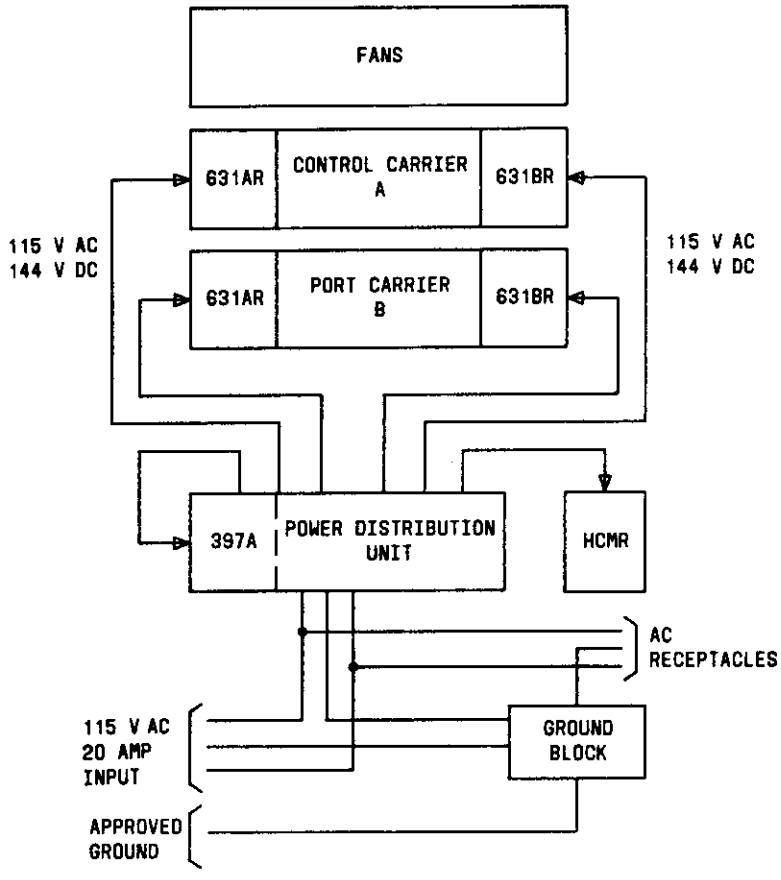

Figure 25. Power Distribution Scheme for 2-Carrier Cabinets

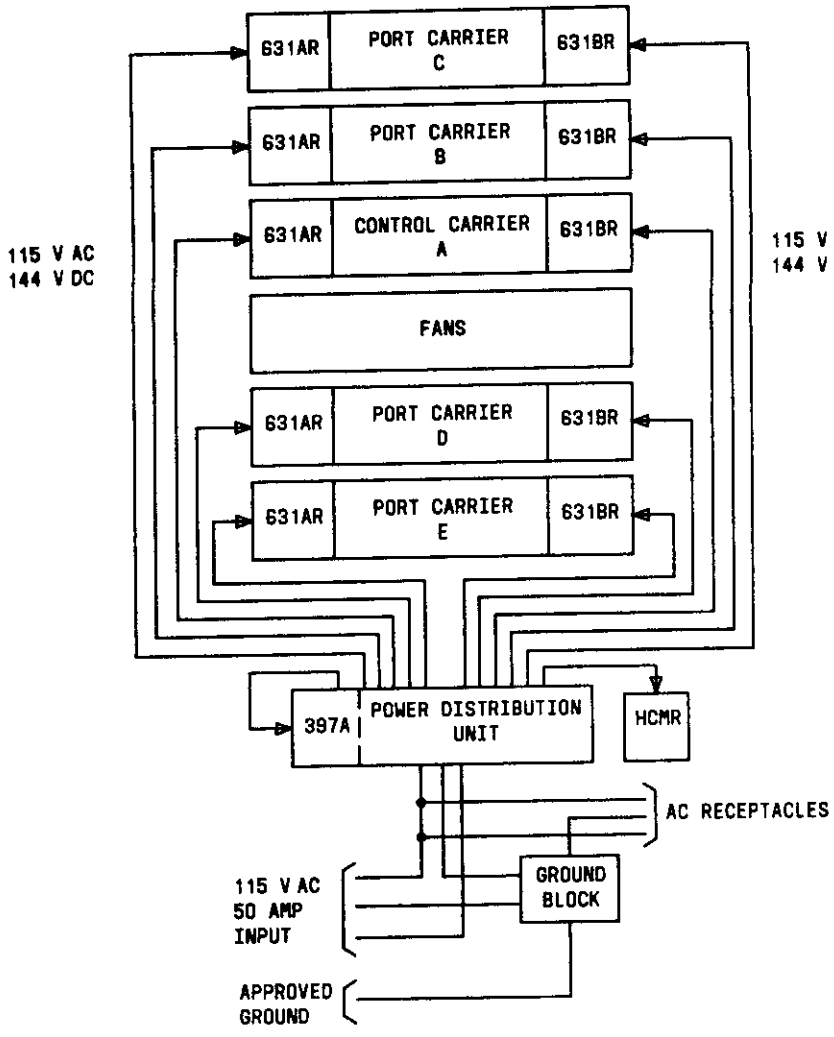

Figure 26. Power Distribution Scheme for 5-Carrier Cabinets

AC Power

The ac input power is distributed using terminal strips to the power distribution cables. Four EMI filters suppress ac line voltage noise. The ac power on the power distribution cables is fused at 20 amps on the 5-carrier cabinet. It is not fused on the 2-carrier cabinet.

Both cabinets contain four ac receptacles (two in front and two in rear). One of the ac receptacles on the rear is used to power the SAT.

Battery Backup

Figure 27 shows the battery backup circuit. The battery backup consists of the following:

- Three 48-volt batteries
- Load switch
- Battery charger

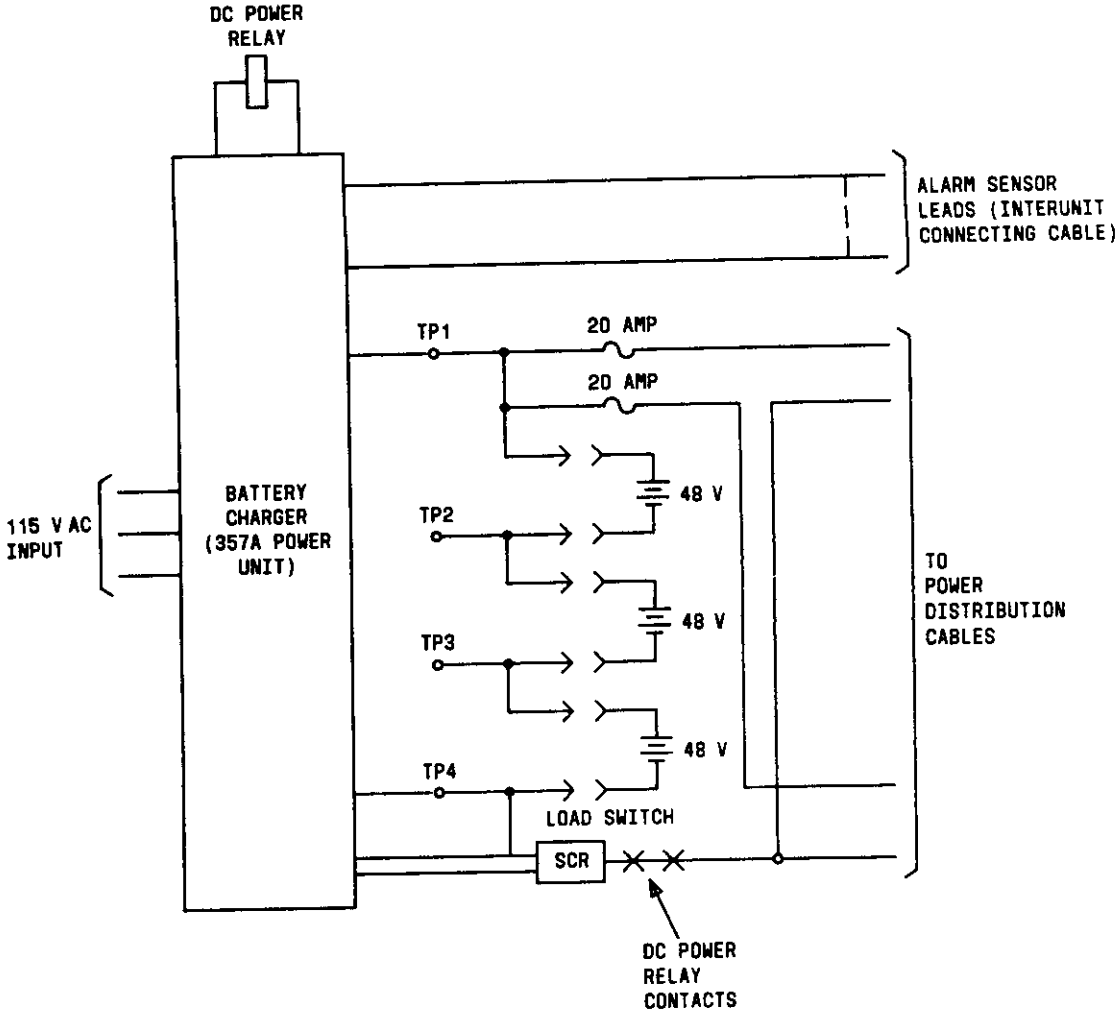

Figure 27. Battery Backup Circuit

Batteries: Power required for operating the system during emergency transfer is provided by three 48-volt dc batteries. The 144-volt dc power is fused at 20 amps. These batteries power the entire system for approximately 10 seconds. They power the control carrier for approximately 10 minutes.

Load Switch: The load switch is a silicon-controlled rectifier (SCR) and two dc power relay contacts connected in series. It provides the disconnect and reconnect of the batteries under control of the battery charger (397A power unit).

Battery Charger: The battery charger provides a dual-rate constant current (5 to 125 ma) to fully charge and float the three 48-volt batteries. The high charge rate mode starts when the battery voltage is below a predetermined level and is maintained until the batteries are fully charged. The charger then transfers automatically to the low charge rate.

An ac monitor circuit informs the charger controller of an ac failure and ac return so that the appropriate signals for battery reserve transfer and disconnect are sent to the load switch. A low-level battery sense circuit disconnects the battery to prevent battery cell reversal during a prolonged power outage. A high-voltage clamp circuit protects against overvoltage conditions and sends a reserve fault alarm to the Maintenance circuit pack.

Alarm information for the battery backup circuit is provided to the Maintenance circuit pack on the interunit connecting cable. These leads indicate the following alarm conditions:

- High-rate charge—Battery charger is operating in the high-rate mode.
- Unit on reserve—AC input voltage is low, and the loads are connected to the batteries.
- Reserve fault—One or more of the following faults is present in the battery backup circuit:
    a. Battery voltage is abnormally high (197 to 220 volts).
    b. Battery charger circuit breaker has operated.
    c. Battery charger is not delivering current due to an internal fault.
    d. Battery charger has operated for 30 hours in the high-rate mode.
- Prepare to die—Battery voltage has dropped to 120 volts and battery disconnect is eminent.
- Emergency shutdown—Battery is disconnected because of the following:
    a. The battery voltage falls below 110 volts.
    b. A battery disconnect signal is received from the SPE.
    c. The circuit breaker on the front of the charger is set to OFF.

The LED on the front of the battery charger lights when a reserve fault condition listed above exists.

124B Frequency Generator

The 124B frequency generator is a dc-to-ac inverter that converts a -48 volt dc input to 75- to 100-volt 20-Hz outputs. The interunit connecting cable provides the input from the 631BR Power Unit located in the control carrier. The interunit connecting cable distributes the outputs to all of the carriers.

The analog port circuit packs use the outputs to provide ringing to their associated voice terminals. Ringing voltage can be applied to a maximum of four ports per analog port circuit pack at any one point in time.

Power Units

631AR Power Unit

The 631AR power unit provides +5 volt dc 60 amp power on the backplane of the carriers for the port and control circuit packs. During normal operation, the power unit converts the 115-volt ac input to +5 volt dc outputs. During an ac power failure, the power unit converts the -144 volts dc supplied by the batteries to +5 volt dc outputs. The power unit contains a relay circuit that detects the highest equivalent input voltage (ac or dc) and switches to the correct converter path accordingly.

The dual-color LED on the front of the circuit pack lights green when the input and output voltages are within tolerances. It lights red for the following conditions:

- Output current is too high or too low with respect to the current programming bus shunt resistance
- Output voltage is below 4-volts dc or above 6-volts dc

The circuit breaker on the front of the circuit pack has no purpose in a System 75 application and should be left in the ON position.

631BR Power Unit

The 631BR power unit provides -48 volt dc 6 amp power on the backplanes of the carriers for the port circuit packs. The control carrier contains one 631BR power unit to power the fans and the packs in slots 11 through 20. Each port carriers also contains one 631BR power unit.

During normal operation, the power unit converts the 115-volt ac input to -48 volt dc outputs. During an ac power failure, the power unit converts the -144 volts dc supplied by the batteries to -48 volt dc outputs. The power unit contains a relay circuit that detects the highest equivalent input voltage (ac or dc) and switches to the correct converter path accordingly.

The dual-color LED on the front of the circuit pack lights green when the input and output voltages are within tolerances. It lights red for the following conditions:

- Recycle command received from SPE
- Output voltage is below 38 volts dc or above 58 volts dc

The circuit breaker on the front of the circuit pack has no purpose in a System 75 application and should be left in the ON position.

TN736 Power Converter

The TN736 Power Converter circuit pack provides -5 volts dc on the backplanes of the control carrier and the port carriers for the port circuit packs.

The Power Converter circuit pack is a dc/dc converter. It contains two identical power supplies that convert the -48 volts dc on the backplane to two -5 volt dc outputs.

Five test points on the front of the circuit pack provide access to backplane voltages (see below).

Test Point	Measurement
48	-48 volts dc
5P	+5 volts dc
5M1	-5 volts dc from power supply one
5M2	-5 volts dc from power supply two
C	Common or ground point

Three LEDs on the front of the circuit pack provide indication of the status of the circuit pack (see below).

LED	Lighted Indication
Yellow	Normal operation
Red	Output voltage of one of the power supplies is below -3 volts dc
Green	Not used

SYSTEM SOFTWARE

The System 75 software consists of the switched services software, administration software, and maintenance software. This software runs on top of the real-time operating system software.

SWITCHED SERVICES SOFTWARE

The switched services software provides the call (switched voice and data) services, the message and display services, and other terminal services. The software resides in the SPE, the Interface 2 circuit pack (when provided), the two 8-bit microprocessors (A and B) in the Network Control circuit pack, and the 8-bit on-board microprocessors in the port and service circuit packs.

The message and display services of the SPE provide incoming and outgoing call identification, the Leave Word Calling feature, and the interface to AP/A provided Leave Word Calling feature. The terminal services provide programming of abbreviated dialing list entries and terminal display services such as time of day.

The switched services software in the SPE uses the operating system to provide a process based, message passing, execution environment. The operating system scheduler provides SPE scheduling for the software according to process priority, activated by message dispatching.

The software in the Interface 2 circuit pack provides the protocol support for the communications link between the AP/A and the SPE. The Interface 2 software also translates between the System 75 commands and the format the AP/A accepts.

Step-By-Step Call Description

The following is a step-by-step description of a call originated by a System 75 digital voice terminal to another System 75 digital voice terminal. Calls originated by other type voice terminals or incoming calls on trunk circuits are similar. In the following description, the 8-bit microprocessor A on the Network Control circuit pack is referred to as the network controller. The 8-bit microprocessors on the port and service circuit packs are referred to as port controllers.

1. The network controller continually polls the port controllers on the port and service circuit packs.
2. The Digital Line port controller detects the terminal user lifting the receiver.
3. The Digital Line port controller sends an off-hook uplink message to the network controller.
4. The network controller deposits the off-hook message in its dual-port RAM.

5. The SPE software retrieves the message and interprets it as a call origination.
6. The SPE sends downlink messages to the network controller.
    a. The first set of messages instruct the originating port on the Digital Line circuit pack to listen for dial tone on a dedicated time slot and to light the call appearance status lamp on the terminal.
    b. The second set of messages instruct the originating port to talk on an available time slot. They also instruct a Tone Detector port controller to connect a touch-tone detector. The touch-tone detector interprets each individual touch-tone digit as it is dialed.
7. When the terminal user dials the first digit, the Digital Line port circuit converts the analog touch-tone signal to a digital signal and places the digital signal on the previously allocated time slot for that port.
8. The touch-tone detector, listening on the same time slot, interprets the tone. The Tone Detector port controller sends a digit up-link message via the network controller to the SPE.
9. The SPE sends a downlink message to the Digital Line port controller instructing it to remove dial tone from the port circuit.
10. The SPE analyzes the first digit, determines that the call is being placed to another System 75 extension, and starts collecting digits.
11. When the SPE collects enough digits to identify an extension (as specified in translations), it discontinues collecting digits.
12. The SPE recognizes that the called extension is a digital voice terminal (see Note) and sends a downlink message to the appropriate Tone Detector port controller to disconnect its touch-tone detector from the time slot.

    Note: If the extension number dialed is invalid, the SPE sends a message to the Tone/Clock port controller to place intercept tone on the time slot assigned to the originating port. Go to Step 20.

13. The SPE determines if there is an available call appearance for the called digital voice terminal user and sends a message to the Tone/Clock port controller to place audible alerting or busy tone, as appropriate, on the time slot assigned to the originating port. Go to Step 20 for busy tone.
14. The SPE sends a downlink message via the network controller to the Digital Line port controller associated with the called extension to turn on the ringer and to flash a call appearance lamp on the called party's digital voice terminal.
15. When the called party lifts the receiver, the Digital Line port controller sends an off-hook message to the SPE as before.
16. The SPE interprets the off-hook message as an answer.
17. The SPE sends downlink messages to the Digital Line port controller to turn off the ringer and to light a call appearance lamp steady on the called party's digital voice terminal.
18. The SPE then sends downlink messages to the Digital Line port controller associated with the answering party to talk on an available time slot and to listen on the time slot assigned to the calling party.
19. The SPE instructs the Digital Line port controller associated with the called party to listen on the time slot assigned to the calling party for talking.

20. When either of the parties hangs up, the Digital Line port controller sends an on-hook message via the network controller to the SPE.
21. The SPE interprets the on-hook message as the end of the call.
22. The SPE sends downlink messages to the Digital Line port controllers to disconnect the time slot connections and turn off the lamps for the two call appearances.

ADMINISTRATIVE SOFTWARE

The system administration software provides the control for system rearrangement and change via a forms based interface. This software resides in the SPE.

The administration software organizes the translation data for administrable entities in the system into forms that can be viewed and changed at the SAT or by INADS. The forms provide for administering the system, obtaining system traffic measurements, and performing maintenance operations.

The administrative software tests entered data for consistency with data previously entered in order to avoid such errors as the assignment of the same extension number to two voice terminals. An erroneous or inconsistent data entry is disallowed and an error indication is provided.

The administrative software can cause the translation data to be downloaded to the tape located in the HCMR on command. The download operation can also be administered to occur daily.

MAINTENANCE SOFTWARE

The maintenance software contains two levels. A high-level subsystem exists on top of the operating system and a low-level subsystem resides independently of the operating system. The high-level maintenance software resides entirely in the SPE. The low-level maintenance software resides in the SPE and Maintenance circuit pack.

The high-level maintenance software provides the following:

- System initialization and recovery
- Software maintenance
- Dynamic system configuration
- Hardware diagnostics and tests
- Maintenance load regulation

The low-level maintenance software provides the following:

- System boot
- Processor hardware test
- Emergency transfer control

- Post-crash system treatment and recovery

The high-level maintenance software operates during normal system operation. The low-level maintenance software operates with the Maintenance circuit pack software when the system is in a state that it is unable to process calls such as after a system crash (emergency transfer) or during the initial installation.

High-Level Maintenance Software

System Initialization and Recovery

The high-level maintenance software gives the system the ability to recover on its own from serious temporary malfunctions or failures. The following levels of system recovery followed by the equivalent maintenance command are provided:

- Level 1—system boot (reset system 4)
- Level 2—system cold start with translation data loading (reset system 3)
- Level 3—system cold start without translation data loading (reset system 2)
- Level 4—system warm start (reset system 1)
- Level 5—process restart (no maintenance command)

The system boot recovery is the same as the system power-up initialization process and is controlled by the low-level maintenance software. The remaining levels of system recovery are jointly controlled by the low-level and high-level maintenance software.

Level 1: This level is invoked when the system is powered up or when escalated to from a level 2 recovery by the low-level maintenance software. All on-board microprocessors are reset. The operating system, system software, and translation data are loaded from tape.

All established calls and calls in progress are dropped. No new calls are allowed until the recovery is complete. Also, some voice terminal and attendant console features are adversely affected. All messages stored by the Leave Word Calling feature (SPE mode) are lost. All lighted Message Waiting lamps go dark. The following features, if activated, are deactivated:

- Attendant Night Service
- Attendant Trunk Group Control
- Automatic Callback
- Call Forwarding
- Call Park
- Make Busy for Direct Department Calling and Uniform Call Distribution
- Send All Calls

The numbers stored by the Last Number Dialed feature are lost. In addition, any translation data entered since the last translation save will be lost. This includes abbreviated dialing list entries that may have been programmed by users.

Level 2: This level is invoked when escalated to from a level 3 recovery by the low-level maintenance software. This level is the same as the level 1 recovery except the operating system and system software are not loaded from tape.

Level 3: This level is invoked when there is a severe system failure condition. This level is the same as the level 2 recovery except no data is loaded from tape and no features are affected.

Level 4: This level is invoked when there is an operating system failure. All established calls are retained. Some calls in progress may not be completed. No new calls are allowed until the recovery is complete. No data is loaded from tape.

Level 5: This level is invoked when there is a process trapped in the maintenance software, administration software, or switched services software. All established calls are retained. Some calls in progress may not be completed. No data is loaded from tape. See Software Maintenance for more detail.

Software Maintenance

The high-level maintenance software performs a sanity audit on processes in the switched services software, administration software, and maintenance software. This audit detects when processes are in infinite loops or waiting for an event that will never occur.

The sanity audits are performed on a cyclic interval. During the cycle, a query request is sent to each process to be audited. When this query message is received, the process must send a message back to the sanity audit. On receipt of the message, the sanity audit flags that process as sane for that particular cycle of the audit.

At the end of the cycle, the maintenance software analyzes the data accumulated and flags all processes not able to report. If a process is not able to report during an audit cycle, the process is skipped during the next cycle. All sanity flags for processes that reported during the cycle are cleared after the completion of the cycle, prior to the beginning of the next cycle.

If a process fails to report for a predetermined number of audit cycles (different for various processes), the maintenance software can take one of two actions to recover, level 5 or level 4. The recovery action depends on the nature of the failure and the processes involved.

Dynamic System Configuration

Dynamic system configuration is the response of the high-level maintenance software to the placement, insertion, and removal of circuit packs that do not have fixed positions in the carriers. These circuit packs are the port circuit packs, Pooled Modem circuit packs, and Tone Detector circuit packs. The system contains a logical and physical circuit pack configuration table.

The logical table includes the circuit packs required to support the terminal/trunk assignments plus any spare circuit packs installed but not administered. It also includes the Tone Detector circuit packs that are installed.

The physical table includes the port circuit packs and Pooled Modem circuit packs that are actually installed in the system. The physical table differs from the logical table when there are needed (translated) circuit packs missing, and when the wrong circuit pack is present in a slot.

Circuit Pack Insertion: When a port or Pooled Modem circuit pack is inserted, the maintenance action taken depends on whether or not the circuit pack is in the logical table.

If the circuit pack is in the table, its type is checked and if it is correct, tests of its common circuitry and port circuitry are run. Appropriate alarms are cleared. If the circuit pack is not in the logical table, only the common circuitry tests are run. If the tests fail, a warning alarm is raised.

When a Tone Detector circuit pack is inserted, common circuitry and port circuitry tests are run as long the number of Tone Detectors installed is below the system capacity. System capacity for Tone Detector circuit packs is a fixed parameter and is not administerable.

Circuit Pack Removal/Failure: When a port or Pooled Modem circuit pack is removed or fails in such a manner to appear removed, the maintenance actions depends on whether or not the circuit pack has any ports administered. If the circuit pack is not in use, then the removal/failure is ignored and no alarms are raised. The removal/failure is reported to INADS only if the circuit pack is in use.

When a Tone Detector circuit pack is removed or fails, the ports for that Tone Detector are removed from service. If the number of remaining Tone Detector circuit pack ports is below the administered minimum amount for the system, an alarm is raised. If the remaining number of Tone Detector ports is above that minimum, no alarms are raised for removed circuit packs. Warning alarms may be generated for failed Tone Detector circuit packs even if the number of good Tone Detector ports is above the administered minimum.

Circuit Pack Translations: When trunks or terminals are added to translations for a position that currently has no circuit pack installed, the action is allowed and a warning alarm is raised. The warning alarm is cleared when the circuit pack is inserted. The circuit pack is checked to see that it is the proper type and tests are run as described previously.

When trunks or terminals are added to translations for a position that currently has a circuit pack installed, the action is allowed as long as the trunks or terminals are compatible with the circuit pack installed. The trunks or terminals are tested and brought into service.

Alarms for a circuit pack can be cleared by replacing the circuit pack or by removing the circuit pack and all translations for the circuit pack. Alarms for a circuit pack port can be cleared by moving the trunk or terminal to another port and changing the translations.

Hardware Diagnostics and Tests

The high-level maintenance software provides automatic periodic testing of System 75 hardware and an interface for the AT&T Information Systems technician or client to perform the periodic tests on demand. If required, the high-level maintenance software can also initiate certain potentially disruptive tests that are not performed periodically. The high-level maintenance software also detects in-line errors generated by the system hardware or software.

Errors detected during periodic or demand tests and in-line testing are recorded in the Error Log. Errors that escalate to an alarm condition are recorded in the Alarm Log. The Alarm Log and Error Log and their use in trouble clearing are described under "TROUBLE CLEARING AIDS" in this manual.

The hardware is maintained as a collection of independent units or maintenance objects (MOs). Each MO has its own maintenance plan. The plan includes tests for detecting and diagnosing problems, system recovery, reconfiguration strategies, and repair activities for that MO.

Automatic System Tests (Periodic Tests): There are two types of periodic tests, short and long. The short tests are normally run once each hour. Some long tests are run each 24 hours. These tests can also be run at the SAT or by INADS.

When an error is detected in an MO during a test, tests are run much more frequently on that MO. Either these tests will fail several times in a row and generate an alarm or the tests will pass and remove the MO from further suspicion. Intensive testing is performed on an MO as long as any errors are being detected, whether it is alarmed or not.

Disruptive Tests: These tests are potentially service disruptive and are only run by the high-level maintenance software when some symptom indicates a problem. A comprehensive memory test falls into this category. This test is performed during a reboot after several crashes have occurred.

In-line Detection: MOs perform in-line hardware error detection. Each time an MO is used, additional hardware tests for correct operation. Errors are detected immediately. When an error is detected, it is reported to the high-level maintenance software. The high-level software also performs in-line software error detection. The cyclic redundancy check on control channel messages is an example of in-line software error detection.

Maintenance Load Regulation

The System 75 switched services software has priority over the maintenance software. The high-level maintenance software reduces the amount of periodic testing when there is a large amount of call processing required. Normal periodic testing as described above is resumed when normal call processing activity resumes.

Low-Level Maintenance Software

When the system is first powered up, or restarted from a system level recovery, the low-level maintenance software has control. It loads the operating system from tape, if necessary. The operating system then has control and creates the high-level maintenance software. The high-level maintenance software then starts all of the administrative and switched services software.

The low-level maintenance software also provides a processor hardware sanity test and a memory hardware test. The processor hardware sanity test is described under "SPE Monitoring and GO-TO-SLEEP Control."

TROUBLE CLEARING AIDS

GENERAL

System 75 provides the following trouble clearing aids:

- Alarm Log
- Error Log
- Maintenance Tests
- Facilities Access Test

These aids can be used to identify the following troubles:

- Intermittent
- Applications Processor
- Backplane
- Switch Processing
- TDM Network

ALARM LOG

An entry in the Alarm Log is generated as a result of errors detected on a System 75 MO by automatic system tests, demand tests, and in-line error detection. The high-level software determines if the errors are serious enough or enough errors have occurred to warrant alarm status.

Alarms are retired if the problem is resolved and further maintenance tests indicate the problem no longer exists. Alarms are also retired if the errors causing the alarm have not been reported for a predetermined interval of time.

The Alarm Log is restricted in size. A new entry overwrites the oldest resolved alarm. If there are no such entries, entries older that six minutes are overwritten. If no entry is found to satisfy these two requirements, the alarm is not entered.

The Alarm Log can be displayed on the on-site SAT or remote SAT by INADS. The Alarm Log is described in the *System Maintenance* manual (555-200-105IS).

ERROR LOG

A record of errors detected during automatic system tests, demand tests, and in-line error detection is maintained in the Error Log. The Error Log, like the Alarm Log, is restricted in size. A new entry overwrites the oldest entry. The overwritten entry must be at least six minutes old. If no such entry is found, the error is not entered. The Error Log can be displayed on the on-site SAT or remote SAT by INADS.

Display Form

When the command **display errors** is entered, the Hardware Error Reports form (see Figure 28) is displayed. Options are available as follows. If no options are selected, the entire Error Log is displayed.

- **ERROR TYPE:** Specifies all Error Log entries for a particular error code entry. This option is normally used with a specific equipment type (see below).
- **PERIOD:** Day, hour, and minute of the beginning and end of the period to be displayed. Either, both dates, or no dates can be entered. If no beginning date is entered, the display begins at the earliest time of the existing records. If no end date is entered, the display ends at the current time. If no dates are entered, all entries to the current time are displayed.
- **EQUIPMENT TYPE:** Specifies errors to be displayed for one of the following five equipment types:
  - *Board Number:* Errors for a particular circuit pack by location (B01, for example)
  - *Port:* Errors for a particular port circuit (B0101, for example)
  - *Category:* Errors for a particular equipment category (see Table C)
  - *Extension:* Errors associated with a particular terminal extension number
  - *Trunk (group/member):* Errors associated with a particular trunk group and member number as identified in translations. If no member number is specified, all errors for the trunk group are displayed.

```
display errors                                          Page 1 of 1

                        HARDWARE ERROR REPORTS

    The following options control what errors will be displayed.

       ERROR TYPES

          Error Type:___

       PERIOD ( Day/Hour:Minute )

          From: __/__:__        To:__ /__:__

       EQUIPMENT TYPE (Choose only one, if any, of the following)

                          Board Number:___
                                  Port:_____
                              Category:_____
                             Extension:____
                   Trunk ( group/member ):__/__
```

Figure 28. Hardware Error Reports Form

TABLE C. Hardware Category Entries

Category	Category Description
STATIONS	All voice terminals external to the switch
DATAMOD	All PDMs, Trunk Data Modules, and DTDMs external to the switch
TRUNKS	All trunks external to the switch
STACRK	All voice terminals external to the switch and their associated on-board circuitry
TRKCRK	All trunks external to the switch and their associated on-board circuitry
STABD	On-board circuitry associated with all voice terminals
TRKBD	On-board circuitry associated with all trunks
DETR	Tone Detector circuitry
TONE	Tone/Clock circuitry
MODEM	Pooled Modem circuitry
NETCON	Network Control data and control channels
INFC	Interface 2 circuitry
PROCR	Processor circuitry
MEMORY	Memory circuitry
EXT-DEV	Auxiliary cabinet
TAPE	Tape Control circuitry, Tape Transport, and tape cartridge
ENVIRON	Power supply, batteries, temperature/air flow, AP, and emergency transfer
MBUS	All circuits connected to the M bus
TDM	Network Control circuitry and TDM bus time slots

Display Output

Figure 29 is a typical Error Log display. Information contained on the display is listed under columns as follows:

- **Port:** Physical location of the maintenance object.
- **Mtce Name:** Abbreviated identifying name of the maintenance object.
- **Alt Name:** Extension number for terminals or trunk group number for trunk groups.
- **Err Type:** Numerical error code that identifies the type of problem. A detailed listing of error codes is included under *Error Codes and Aux Data* in this manual.
- **Aux Data:** Additional numerical information (auxiliary data) concerning the error type. Only the most recent auxiliary data related to the error type is displayed. A detailed listing of auxiliary data numbers by error code is included under *Error Codes and Aux Data* in this manual.
- **First Occur:** First day, hour, and minute that this error type was reported.
- **Last Occur:** Day, hour, and minute of the most recent occurrence of this error type.

  Note: If the system is unable to retrieve the time of day when this error type last occurred, "01:43" is displayed.

- **Err Cnt:** A count of the number of times that this error type has occurred.

  Note: If this number is greater than 255, "999" is displayed.

- **Err Rate:** Average hourly rate at which the errors have occurred from the first occurrence to the present.

  Note: If this number is greater than 255, "999" is displayed.

- **Rt/Hr:** Approximation of the rate at which this error occurred in the last hour.

  Note: If this number is greater than 255, "999" is displayed.

- **Alarm Status:** Status of this maintenance object in the Error and Alarm Logs ("n" for not alarmed, "a" for active alarm, and "r" for resolved alarm).
- **Act?:** A flag indicating whether or not the maintenance object is still under active consideration by the maintenance software (yes "y" or no "n").

display errors Page 1

HARDWARE ERROR REPORT

Port	Mtce Name	Alt Name	Err Type	Aux Data	First Occur	Last Occur	Err Cnt	Err Rate	Rt/ Hr	Alarm Status	Act?
B1906	DIG-LINE	2864	513	0	27/18:43	28/09:52	87	5	3	a	y
B1906	DIG-LINE	2864	1025	40965	27/18:43	28/09:52	87	5	3	a	y
B1906	DIG-LINE	2864	1793		27/18:44	27/23:54	12	2	0	a	y
B1905	DIG-LINE	2860	1793		27/18:44	27/18:44	1	0	0	n	n
B1901	DIG-LINE	2849	1793		27/18:44	27/18:44	1	0	0	n	n
C0908	HYB-LINE	2923	1025		28/01:52	28/01:52	1	0	0	n	n
B1607	DIG-LINE	2945	1793		28/02:06	28/02:06	1	0	0	n	n
B1701	DIG-LINE	2846	1793		28/02:10	28/02:10	1	0	0	n	n
B1202	DIG-LINE	2828	1793		28/02:21	28/02:21	1	0	0	n	n
C2008	ANL-LINE	2850	0	0	28/08:52	28/08:52	1	0	1	r	n
C2005	ANL-LINE	2943	0	0	28/08:52	28/08:52	1	0	1	r	n
C2003	ANL-LINE	2932	0	0	28/08:52	28/08:52	1	0	1	r	n
C2001	ANL-LINE	2820	0	0	28/08:52	28/08:52	1	0	1	r	n
C2004	ANL-LINE	2957	0	0	28/08:52	28/08:52	1	0	1	r	n

Figure 29. Typical Error Log Display Output

Error Codes and Aux Data

The following is a list of Error Log error codes and auxiliary data. Descriptions are provided for each error code and auxiliary data entry. The list is preceded by error codes and auxiliary data common to maintenance objects and port circuit packs. The remainder of the list is in alphabetical order according to the "Mtce Name" of the maintenance object.

All Maintenance Objects

Error Type	Description	Aux Data	Description
0	Alarm raised without logging errors.	0	Always the case.
15	Audit request failed.		
18	MO was busied out by craft.		

Common Portion of Port Circuit Packs

Error Type	Description	Aux Data	Description
1	On-board microprocessor sanity failure.		
23	Circuit pack administered but not installed.		
257	Control channel failure.	11	Bad uplink message.
		15	Bad downlink message, one retransmission.
		16	Bad downlink message, no retransmission.
		17	Bad retransmission.
		65535	Control channel loop failure.
513	On-board microprocessor background test error.	4352	External RAM error.
		4353	Internal RAM error.
		4355	ROM checksum error.
		4357	Instruction set error.

769	On-board microprocessor logic error.	4358	Program logic inconsistency.
1025	NPE audit failure.	12800	NPE audit failure.
1281	Ringing application circuit test failed (line circuit only).		
1538	On-board microprocessor is hyperactive.		
3840	Inconsistent downlink message. This error code and the associated aux data are developmental diagnostic messages and should be ignored.	4096	Bad major heading.
		4097	Bad port number.
		4098	Bad data.
		4099	Bad sub-qualifier.

ANL-LINE (Analog Line)

Error Type	Description	Aux Data	Description
1	In-line Errors.	40975	Switchhook error.
		40977	Station is absent.
		40973	Ringing voltage absent.
15	In-line Errors.	1	Switchhook audit failed.
		5	Lamp update failed.
		7	Translation update failed.
		8	Ringer update failed.
257	Ringing Application Station Test Failed.		
513	Battery Feed Test Failed.		
769	Loop around and Conference Test Failed.		
1025	NPE Crosstalk Test Failed.		

AP

Error Type	Description	Aux Data	Description
1	AP Major alarm.		
257	AP Minor alarm.		
513	AP Warning alarm.		

AUX-TRK (Auxiliary Trunk)

Error Type	Description	Aux Data	Description
1	Diagnostic test.	57482	Fault on signaling lead.
		57481	Port Fault.
257	Hybrid/Conference circuit test.		
513	NPE crosstalk test.		

CARR-POW (Carrier Power)

Error Type	Description	Aux Data	Description
1	Carrier supply error.		

CABINET

Error Type	Description	Aux Data	Description
1	Air flow error.		
257	Over temperature.		

CO-TRK (CO Trunk)

Error Type	Description	Aux Data	Description
1	Port Error.	57347	Ringing without ground.
257	Trunk Error.	57408	No tip detected on outgoing call.
		57345	Single polarity ringing current.
		57376	No loop current on incoming call.
		57424	No loop current on outgoing call.
		57360	Ground but no ringing.
513	Detector Stuck.	57364	Ground detector stuck.
769	Loop current active	57392	CO not releasing trunk after PBX disconnect.
766 and 1278	Loop current missing.	57393	CO belated release.
1025	Diagnostic test failure, trunk.		
1281	Diagnostic test failure, port.		
1537	Dial tone seizure test failure.		
1793	Loop around and conference test failure.		
2049	NPE crosstalk test failure.		
2305	Seizure test failed.	57408	No tip detected outgoing call.
		57416	No loop current on outgoing call.

CONFIG (Configuration)

Error Type	Description	Aux Data	Description
0 -> 128	On-board microprocessor X failed to answer board inquiry.		
1000 -> 1128	On-board microprocessor X failed to answer vintage inquiry.		

DATA-CHL (Data Channel)

Error Type	Description	Aux Data	Description
1	Local loopback failed.		
257	Maintenance loopback failed.		
513	Crosstalk test failed.		
769	Dual-port RAM failure.		
1025	Data driver flow control.		

DID-TRK (DID Trunk)

Error Type	Description	Aux Data	Description
16	On-hook timing.	16384	CO began transmitting call digits too late after receiving a PBX wink.
		57476	Rotary dial before wink.
		57477	Rotary dial pulse too early.
		57483	Rotary dial pulse during wink.
288	Digit detection.	57472	Rotary dial break too long.
		57473	Rotary dial rate too slow.
		57474	Rotary dial rate too fast.
		57475	Interdigit time too short.
513	Loop current active.	57392	CO not releasing trunk after PBX disconnect.
766	Loop current missing.	57393	CO belated release.
769	Battery feed test failure.		
1025	Loop around and conference test failure.		
1281	NPE crosstalk test failure.		

DIG-LINE/PDMODULE/TDMODULE

(Digital Line/Processor Data Module/Trunk Data Module)

Error Type	Description	Aux Data	Description
1	Noisy link or port.	40987	Bad scan alarm.
		i	Where i= number of bad scans received by inquiry divided by 15.
257	Trouble transmitting to the station.	40971	Transmit stuck.
513	No response from station to an ID Request (possibly unplugged station).		
769	Short on link or station.	40963	EPF on, overcurrent.
		40988	EPF off.
1025	Station has no power (open circuit or station unplugged).	40965	EPF on, no load.
1281	Station responded to ID Request but health bit is not OK.		Actual value of health bit returned.
1537	Something wrong with link to station.	40968	Link Reset Alarm.
1793	Local loopback.		
2049	NPE crosstalk test failed.		
2305	Off-hook received while station in "ready for service" state (state of inconsistency).		
3840	Should not happen unless firmware problem.	40989	EPF off.

DTMF-PT (Touch-Tone Receiver Port)

Error Type	Description	Aux Data	Description
1	DPS is insane.	17664	DSP insane.
257	Bad port translation.	17666	Bad translation.
513	Tone detector tests failed.		

EMG-XFER (Emergency Transfer)

Error Type	Description	Aux Data	Description
1	Emergency transfer is manual-on.		
257	Emergency transfer is manual-off.		

GPTD-PT (General Purpose Tone Detector Port)
See **DTMF-PT**.

HYB-LINE (Hybrid Line)

Error Type	Description	Aux Data	Description
1	Noisy link or port.	40987	Bad Scan Alarm reported by board.
		i	Where i= Bad scan count received by inquiry divided by 10.
257	Short on link to station.	40963	EPF on, overcurrent.
		40988	EPF off.
513	Station has no power (open circuit or unplugged station).	40965	EPF on, no load.
769	Remote station test failed.		
1025	Hybrid test or conference test failed.		
1281	Local digital loop around test failed.		
1537	Something wrong with link to station.	40968	Link Reset Alarm.
1793	NPE crosstalk test failed.		
2049	"Off-hook" received while in "ready for service" state (state of inconsistency).		
3840	Should not happen unless firmware problem.	40989	EPF off.

INTFC2 (Interface 2)

Error Type	Description	Aux Data	Description
0	INTFC2 downloaded by request.	0	
1		0	Download of INTFC2 occurred from tape.
257	S bus check failed.		
513	INTFC2 memory handshake failure.		
769	INTFC2 message handshake failure.	30001	No reply received before timeout.
		30002	Data in reply message incorrect.
		30003	Cannot open S bus.
1001	INTFC2 error log.	1001	S bus parity error.
1002	INTFC2 error log.	1002	S bus access error.
1003	INTFC2 error log.	1003	Breakpoint NMI.
1004	INTFC2 error log.	1004	Halt instruction hit.
1005	INTFC2 error log.	1005	Interface 2 Timeout NMI.
1006	INTFC2 error log.	1006	Interface 2 sanity timeout.
1007	INTFC2 error log.	1007	Interface 2 parity error.
1008	INTFC2 error log.	1008	Interprocessor NMI.
1009	INTFC2 error log.	1009	PBEE NMI.
1010	INTFC2 error log.	1010	RTX panic.
1011	INTFC2 error log.	1011	Stray interrupt.
1012	INTFC2 error log.	1012	BX.25, out of paths.
1013	INTFC2 error log.	1013	BX.25, no LNC buffers.
1014	INTFC2 error log.	1014	BX.25, no AI buffers.
1015	INTFC2 error log.	1015	BX.25, no command buffers.
1016	INTFC2 error log.	1016	BX.25, no message buffers.

1017	INTFC2 error log.	1017	No status from BX.25.
1018	INTFC2 error log.	1018	Alarm, unable to send to LNC.
1019	INTFC2 error log.	1019	Alarm, unable to send to SL.
1020	INTFC2 error log.	1020	Alarm, unable to send to ap_high.
1021	INTFC2 error log.	1021	Alarm, unable to send to ap_low.
1022	INTFC2 error log.	1022	Queue count inconsistent.
1023	INTFC2 error log.	1023	RTX run queue inconsistent.
1024	INTFC2 error log.	1024	Bad checksum.
1025	INTFC2 error log.	1025	Interface 3 control dual-port RAM bad.
1026	INTFC2 error log.	1026	Interface 3 data dual-port RAM bad.
1027	INTFC2 error log.	1027	Illegal protocol module input.

MAINT (Maintenance)

Error Type	Description	Aux Data	Description
1	Background fault.	3585	Background bad ROM checksum.
		3586	Background bad ROM locations(s).
		3841	RTX logical inconsistency.
		3842	Bad port circuit microprocessor start-up message.
257	Driver fault.	0	MB control driver fault.
		8	MB is stuck asleep.
		256	MB data driver port 0 fault.
		257	MB data driver port 1 fault.
513	DSP disconnect.		
769	Dual-port RAM fault.	4	No case for rcv-spe message.
		5	Bad dual-port RAM pointer.
1025	Single polarity ringing.		

MBUF (Message Buffer)

Error Type	Description	Aux Data	Description
10	Kernel notification.	1	Level 2 watermark reached.
		2	Level 1 watermark reached.
		3	High watermark reached.

MEMORY

Error Type	Description	Aux Data	Description
0-30	Single bit memory error.		
257	Multiple bit memory error.		
513	Memory error detection/correction circuit error.		
769	RAM checksum test failed.		
1025	Text or data checksum error on reboot (unresolvable with out rebooting again).		

MODEM-PT (Pooled Modem Port)

Error Type	Description	Aux Data	Description
1	Short calls.		
257	Loop around test failed.		
513	Conference test failed.		
769	NPE crosstalk test failed.		

OPSYS (Operating System)

Error Type	Description	Aux Data	Description
20	Process manager notification.	8	PM_KILL.
		6	PM_SUICIDE.
		7	PM_TRAP.

OVERLOAD
The aux data for all error types is zero.

Error Type	Description	Aux Data	Description
13	Level 2 watermark on message buffers reached.		
12	Level 1 watermark on message buffers reached.		
14	High watermark on message buffers reached.		
16	Level 2 watermark on path records reached.		
15	Level 1 watermark on path records reached.		
17	High watermark on path records reached.		

PATH-DES

Error Type	Description	Aux Data	Description
10	Kernel notification.	1	Level 2 Watermark reached.
		2	Level 1 Watermark reached.
		3	High watermark reached.

PDMODULE (Processor Data Module)
See **DIG-LINE**.

POWER

Error Type	Description	Aux Data	Description
1	Reserve fault.		
257	High charging rate.		
513	No ac.		
769	Low battery voltage.		

PROC-BD (Processor Circuit Pack)

Error Type	Description	Aux Data	Description
1	Software initiated interrupt test failed.		
257	Memory management circuit test failed.		
513	Stack overflow/scratchpad RAM test failed.		
769	ROM checksum test failed.		
1025	NMI test failed.		
1281	Sanity timer test failed.		

PROC-SAN (Process Sanity)

No errors reported. If a process is reset, it is logged under the MO name for that process.

SW-CTL (Network Control)

Error Type	Description	Aux Data	Description
1	Massive microprocessor B failure.		
2	Fail control channel integrity test.		
257	Fail microprocessor A background memory test.	0	ROM failure.
		1	RAM failure.
513	Fail time-of-day short term accuracy test.		
769	TDM bus clock failure.		
1025	Fail microprocessor A loop around test.		
1281	Microprocessor A handshake failure.		Handshake counter value.
1537	Microprocessor A reset.		
1793	Apparent dual-port RAM failure (many causes).		Port ID of failed message.
2049	Fail time-of-day long term accuracy test.		
2305	Driver error reporting flow control.		
2561	DCP clock failure.		

SYSTEM

The "Aux Data" field may be zero or the return code from a bad kernel call, but these examples in no way exhaust the possibilities.

Error Type	Description	Aux Data	Description
10	Warm start performed.		
8	Cold start level I performed.		
9	Cold start lever II performed.		
602	Escalate the restart level to Cold I.		
601	Error encountered during initialization.		

TAPE

Aux data: The error word indicates which of the following errors occurred by the corresponding bit being set.

Error Word
==========

Bit	Error
0	no cartridge
1	write protected
2	cmd timeout
3	bus not enable
4	self-test error
5	parity error
6	tape motion error
7	unable to write
8	illegal command
9	block number err
10	err in block header
11	correctable err
12	reread was done
13	rewrite was done
14	unable to locate blk
15	unable to open

Error Type	Description	Aux Data	Description
1	No tape cartridge.		Error word.
257	Tried to write protected area.		
513	Tape Control loopback test failed.		Tape Control return code.
769	I/O buffer test failed.		Tape Control return code.
1025	Command timeout of buffer disabled.		Error word.
1281	Tape firmware self-test failed.		Error word.
1537	HCMR failed tape diagnostic test.		Tape Control return code.
1793	Cartridge failed diagnostic test.		Tape Control return code.
2049	Tape motion error, unable to write, illegal command, block number error, or parity error.		Error word.

2305	Error in block header, correctable error, reread was done, rewrite was done, unable to locate block, or unable to open.	Error word.
2561	Uncorrectable error.	Error word.
2562	Low-level maintenance reports bad copy.	Error word.
2817	Tape ID mismatch.	Error word.
3329	Error reading translation.	Tape manager return code.

TDMODULE (Trunk Data Module)
see **DIG-LINE**

TDM-BUS

Error Type	Description	Aux Data	Description
X	X bad time slots detected.		

TIE-TRK (Tie Trunk)

Error Type	Description	Aux Data	Description
1	On-hook timing.	57485	Wink too short for valid signal.
		57476	On-hook before wink.
		57477	On-hook before ready to receive digits.
257	Digit detection.	57472	Rotary dial break too long.
		57473	Rotary dial rate too slow.
		57474	Rotary dial rate too fast.
		57475	Interdigit time too short.
513	Off board line error.	57478	EPF overload
		57480	EPF no load.
769	Port fault.	57481	On-board EPF failure.
1025	No external PBX disconnect.	57392	Other PBX did not disconnect.
1281	E and M lead failure.		
1537	Loop around and conference tests.		
1793	Seizure test.		
2049	NPE crosstalk test.		

TONE-PT (Tone/Clock Port)

Error Type	Description	Aux Data	Description
1	DSP is insane.	17664	DSP insane.
257	Dual port RAM error.	17667	Dual port RAM error.
513	Bad port translation.	17666	Bad translation.
769	Tone generator transmission tests failed.		
1025	Crosstalk test failed.		
1281	Bus clocks failed.		
1537	DCP clocks failed.		

TTR-LEV
(Touch-Tone Receiver and Call Progress Tone Receiver Level)

Error Type	Description	Aux Data	Description
0	TTR levels above threshold.		
1	TTR levels below threshold.		
2	CPTR levels above threshold.		
3	CPTR levels below threshold.		

MAINTENANCE COMMANDS

Maintenance commands entered at the SAT or by INADS provide a means of demand testing maintenance objects in the system. The commands are classified as follows:

- Test
- Reset
- Busyout
- Release
- Display
- Miscellaneous

Error codes are provided in the test results for test, reset, busyout, and recycle commands.

Test Commands

The test commands (except "test led" command described under *Miscellaneous Commands* cause tests to be run on the System 75 maintenance objects. The short tests are the tests that the maintenance software automatically runs each hour. The long tests are basically those tests that the maintenance software automatically runs each 24 hours. When the long test is specified, the short tests are run also. The tests can be repeated as required.

The test results are displayed on the SAT or at INADS. Figure 30 is an example of typical test results. The following information is contained in the test results:

- **Port:** Physical location of the maintenance object—carrier, slot number, port number

  Note: This information does not apply to fixed position circuit packs.

- **Maintenance Name:** Logical name of the maintenance object
- **Test No.:** A system identifying number for the individual tests
- **Result:** The results of the individual test—pass, fail, or abort

  Note: All tests for a port on an intelligent port circuit pack abort if that port is busy.

- **Error Code:** A system generated number that tells why the individual test failed or aborted. A detailed list of the codes according to "Test No." is provided under *Error Codes* in this manual.

```
test port B1905 long

                                TEST RESULTS

Port        Maintenance Name    Test No.    Result      Error Code

B1905       DIG-LINE            9           PASS
B1905       DIG-LINE            11          PASS
B1905       DIG-LINE            13          PASS
B1905       DIG-LINE            16          PASS
B1905       DIG-LINE            17          PASS
```

Figure 30. Typical Demand Test Results

A definition of the test commands according to maintenance object is provided in the following order:

- Common Intelligent Port Circuit Pack Tests
- Analog Voice Terminal/Port
- Hybrid Voice Terminal/Port
- MET Voice Terminal/Port
- Digital Voice Terminal/Port
- CO Trunk Group/Trunk
- DID Trunk Group/Trunk
- TIE Trunk Group/Trunk
- Auxiliary Trunk Group/Trunk
- Pooled Modem
- Tone Detector
- Tone/Clock
- Network Control
- Data Channel
- Processor
- Memory
- AP Interface
- Tape
- Maintenance
- Environment

Individual tests for ports/terminals are listed in the order performed. Long port/terminal tests are performed and then the short tests. The sequence of the other tests vary according to the type of test requested (short or long) and are listed separately.

A list of test commands according to maintenance object follows:

COMMON INTELLIGENT PORT CIRCUIT PACK TESTS

Command: **test board** "qualifier" **short/long r** (No.)

Qualifier: Circuit pack location for intelligent port circuit pack (b01, for example)

Short Tests:

The following tests are run in the order listed (when applicable) followed by the short terminal/port tests. Test No. 51 applies only to the Analog Line circuit pack.

- Test No. 51 (Ringing Application Test)
- Test No. 52 (Control Channel Loop Around Test)

Long Tests:

The following tests are run in the order listed (when applicable) followed by the long and short terminal/port tests. Test No. 51 applies only to the Analog Line circuit pack.

Note: All associated calls for the tested circuit pack are destroyed.

- Test No. 52 (Control Channel Loop Around Test)
- Test No. 51 (Ringing Application Test)
- Test No. 50 (NPE Audit)
- Test No. 53 (SAKI Reset Test)

ANALOG VOICE TERMINAL/PORT

Command: **test station port** "qualifier" **short long r** N

Qualifier: Terminal extension number or port location (b0101, for example)

Long Tests Only:

- Test No. 6 (NPE Crosstalk Test)
- Test No. 47 (Hybrid and Conference Test)

Short Tests:

Note: If Test No. 48 fails, Test No. 36 is not performed.

- Test No. 35 (Port Diagnostic Test)
- Test No. 48 (Ringing Application Test)
- Test No. 36 (Audit Update)

HYBRID VOICE TERMINAL/PORT

Command: **test station/port** "qualifier" **short/long r** (No.)

Qualifier: Terminal extension number or port location (b0101, for example)

Long Tests Only:

Note: If test No. 58 fails, no short tests are performed.

- Test No. 6 (NPE Crosstalk Test)
- Test No. 56 (EPF Restoral Test)
- Test No. 57 (Hybrid Circuit and Conference Test)
- Test No. 58 (Digital Loop Around Test)

Short Tests:

Note: If Test No. 59 fails, the remaining tests are not performed.

- Test No. 59 (Remote Station Test)
- Test No. 60 (Station Lamp Updates)
- Test No. 61 (Station Audits)
- Test No. 62 (Ringer Update)

MET VOICE TERMINAL/PORT

Command: **test station/port** "qualifier" **short/long r** (No.)

Qualifier: Terminal extension number or port location (b0101, for example)

Long Tests Only:

- Test No. 6 (NPE Crosstalk Test)
- Test No. 56 (EPF Restoral Test)
- Test No. 57 (Hybrid Circuit and Conference Test)

Short Tests:

Note: If Test No. 59 fails, the remaining tests are not performed.

- Test No. 59 (Remote Station Test)
- Test No. 60 (Station Lamp Updates)
- Test No. 61 (Station Audits)
- Test No. 62 (Ringer Update)

DIGITAL VOICE TERMINAL/PORT

Command: **test station/port** "qualifier" **short/long r** (No.)

Qualifier: Terminal extension number or port location (b0101, for example)

Long Tests Only:

- Test No. 9 (NPE Crosstalk Test)
- Test No. 11 (EPF Restoral Test)
- Test No. 13 (Voice and Control Channel Local Loop Test)

Short Tests:

- Test No. 16 (Station Lamp Updates)
- Test No. 17 (Station Audits)

CO TRUNK GROUP/TRUNK

Command: **test trunk** "qualifier" **short/long r** (No.)

Qualifier: Trunk group number, or trunk group number and member number, or port location (b0101, for example). If the trunk group number only qualifier is entered, the following tests are performed for all the trunks in the group (maximum of four).

Long Tests Only:

- Test No. 6 (NPE Crosstalk Test)
- Test No. 33 (Loop Around and Conference Test)
- Test No. 0 (Dial Tone Test)

Short Tests:

- Test No. 3 (Diagnostic Test)
- Test No. 36 (Audit Update)

DID TRUNK GROUP/TRUNK

Command: **test trunk** "qualifier" **short/long r** (No.)

Qualifier: Trunk group number, or trunk group number and member number, or port location (b0101, for example). If the trunk group number only qualifier is entered, the following tests are performed for all the trunks in the group (maximum of four).

Long Tests Only:

- Test No. 6 (NPE Crosstalk Test)
- Test No. 33 (Loop Around and Conference Test)

Short Tests:

- Test No. 35 (Port Diagnostic Test)
- Test No. 36 (Audit Update)

TIE TRUNK GROUP/TRUNK

Command: **test trunk** "qualifier" **short/long r** (No.)

Qualifier: Trunk group number, or trunk group number and member number, or port location (b0101, for example). If the trunk group number only qualifier is entered, the following tests are performed for all the trunks in the group (maximum of four).

Long Tests Only:

- Test No. 6 (NPE Crosstalk Test)
- Test No. 33 (Loop Around and Conference Test)

Short Tests:

- Test No. 73 (Seizure Test)
- Test No. 74 (Electronic Power Feed Test)
- Test No. 36 (Audit Update)

AUXILIARY TRUNK GROUP/TRUNK

Command: **test trunk** "qualifier" **short/long r** (No.)

Qualifier: Trunk group number, or trunk group number and member number, or port location (b0101, for example). If the trunk group number only qualifier is entered, the following tests are performed for all the trunks in the group (maximum of four).

Long Tests Only:

- Test No. 6 (NPE Crosstalk Test)
- Test No. 33 (Loop Around and Conference Test)

Short Tests:

- Test No. 114 (Diagnostic Test)
- Test No. 36 (Audit Update)

POOLED MODEM

Command: **test board/pooled-modem** "qualifier" **short/long r** (No.)

Qualifier: Pooled Modem circuit pack location (b01, for example) required only for the "board" test. The "pooled-modem" test causes all Pooled Modems in the system to be tested and does not require a qualifier.

> ***Note:*** The following tests are repeated for both modems on the Pooled Modem circuit pack(s).

Long Tests Only:

- Test No. 96 (Modem NPE Crosstalk Test)
- Test No. 97 (Modem Conference Test)

Short Tests:

- Test No. 98 (Conversion Resource Loop Around Test)
- Test No. 99 (Modem Audits)

TONE DETECTOR

Command: **test board** "qualifier" **short/long r** (No.)

Qualifier: Tone Detector circuit pack location (a03, for example).

Long Tests:

Note: Test No. 42 and 43 are repeated for each general purpose tone detector port (two) and each touch-tone port (four).

- Test No. 42 (Tone Detection Test)
- Test No. 43 (Tone Detector Audit/Update)
- Test No. 52 (Control Channel Loop Around Test)
- Test No. 50 (NPE Audit)
- Test No. 53 (SAKI Reset Test)

Short Tests:

Note: Test No. 42 and 43 are repeated for each general purpose tone detector port (two) and each touch-tone port (four).

- Test No. 42 (Tone Detection Test)
- Test No. 43 (Tone Detection Audit/Update)
- Test No. 52 (Control Channel Loop Around Test)

TONE/CLOCK

Command: **test tone-clock short/long r** (No.)

Long Tests:

Note: In-progress calls may be disrupted by Test No. 53.

- Test No. 90 (Tone Generator Crosstalk Test)
- Test No. 40 (Tone Generator Transmission Test)
- Test No. 41 (Tone Generator Audit/Update)
- Test No. 52 (Control Channel Loop Around Test)
- Test No. 53 (SAKI Reset Test)

Short Tests:

- Test No. 40 (Tone Generator Transmission Test)
- Test No. 41 (Tone Generator Audit/Update)
- Test No. 52 (Control Channel Loop Around Test)

TDM BUS

Command: **test tdm short/long r** (No.)

Note: The long and short test are identical for the TDM bus.

Test:

- Test No. 4 (Idle Time Slot Test)

NETWORK CONTROL

Command: **test network-control short/long r** (No.)

Long Tests:

Note: Tests No. 107, 108, 109, 110, and 111 are repeated for each of the four data channels. In-progress calls may be disrupted by Test No. 53.

- Test No. 52 (Control Channel Loop Around Test)
- Test No. 50 (NPE Audit)
- Test No. 53 (SAKI Reset Test)
- Test No. 107 (Data Channel Reset)
- Test No. 108 (Dual-Port RAM Test)
- Test No. 109 (Maintenance Loop Around Test)
- Test No. 110 (Data Channel Crosstalk Test)
- Test No. 111 (Data Channel Local Loopback Test)
- Test No. 93 (8-Bit On-Board Microprocessor A Reset Test)
- Test No. 95 (Time-of-Day Clock Test)
- Test No. 92 (8-Bit On-Board Microprocessor A Loop Around Test)
- Test No. 94 (Control Channel Integrity Test)

Short Tests:

Note: Tests No. 109, 110, and 111 are repeated for each of the four data channels.

- Test No. 52 (Control Channel Loop Around Test)
- Test No. 109 (Maintenance Loop Around Test)
- Test No. 110 (Data Channel Crosstalk Test)
- Test No. 111 (Data Channel Local Loopback Test)
- Test No. 92 (8-Bit On-Board Microprocessor A Loop Around Test)
- Test No. 94 (Control Channel Integrity Test)

Command: **test data-channel** "qualifier" **short/long r** (No.)

Qualifier: Data channel number (1—4)

Long Tests:

Note: All data channels are disrupted by the following tests.

- Test No. 107 (Data Channel Reset)
- Test No. 108 (Dual-Port RAM Test)
- Test No. 109 (Maintenance Loop Around Test)
- Test No. 110 (Data Channel Crosstalk Test)
- Test No. 111 (Data Channel Local Loopback Test)

Short Tests:

Note: Data channels are tested in pairs. Testing data channel 1 or data channel 2 disrupts both data channel 1 and 2. Testing data channel 3 or 4 will disrupt both data channel 3 and 4.

- Test No. 109 (Maintenance Loop Around Test)
- Test No. 110 (Data Channel Crosstalk Test)
- Test No. 111 (Data Channel Local Loopback Test)

PROCESSOR

Command: **test processor short/long r** (No.)

Long Tests:

Note: The following tests cause a system reboot. All calls are disrupted.

- Test No. 77 (Software Initiation Interrupt)
- Test No. 78 (Memory Management On/Off)
- Test No. 79 (Overflow Stack)
- Test No. 80 (ROM Checksum)
- Test No. 82 (Non-Maskable Interrupt Test)
- Test No. 83 (Sanity Timer)

Short Tests:

- Test No. 77 (Software Initiation Interrupt)
- Test No. 78 (Memory Management On/Off)
- Test No. 79 (Overflow Stack)
- Test No. 80 (ROM Checksum)
- Test No. 82 (Non-Maskable Interrupt Test)

MEMORY

Command: **test memory short/long r** (No.)

Long Tests:

- Test No. 85 (Memory Read All Test)
- Test No. 86 (RAM Checksum)
- Test No. 87 (Memory Error Detection)

Short Tests:

- Test No. 87 (Memory Error Detection)

APPLICATIONS PROCESSOR INTERFACE

Command: **test interface short/long r** (No.)

> ***Note:*** This command tests the application processor link, not all three interface circuit packs.

Long Tests:

- Test No. 119 (S Bus Check)
- Test No. 118 (Interface 2 Read Status)
- Test No. 116 (Interface 2 Handshake)

Short Tests:

- Test No. 118 (Interface 2 Read Status)
- Test No. 116 (Interface 2 Handshake)

TAPE

Command: **test tape short/long r** (No.)

Note: This command tests Tape/Control circuit pack, the tape drive, and the tape cartridge.

Long Tests:

Note: The following tests take approximately 45 minutes to run.

- Test No. 64 (HCMR Read Test)
- Test No. 65 (HCMR Read/Write Test)
- Test No. 66 (HCMR Diagnostic Test)
- Test No. 67 (HCMR Buffer Test)
- Test No. 68 (HCMR Loopback Test)
- Test No. 69 (HCMR Status Test)

Short Tests:

- Test No. 66 (HCMR Diagnostic Test)
- Test No. 67 (HCMR Buffer Test)
- Test No. 68 (HCMR Loopback Test)
- Test No. 69 (HCMR Status Test)

Command: **test maintenance short/long r** (No.)

Note: The long tests for this command are different for a remote SAT and are listed first. The short tests are the same for a remote SAT and the SAT connected directly to the Maintenance circuit pack.

Long Tests (Remote SAT):

- Test No. 101 (Reset Test)
- Test No. 102 (Outpulse Relay Test)
- Test No. 103 (Analog Loop Test)
- Test No. 104 (Dual-Port RAM Test)
- Test No. 106 (Sanity Handshake)

Long Tests (Dedicated SAT):

- Test No. 101 (Maintenance Circuit Pack Reset Test)

  Note: The SAT is logged off.

Short Tests:

- Test No. 102 (Outpulse Relay Test)
- Test No. 103 (Analog Loop Test)
- Test No. 106 (Sanity Handshake)

ENVIRONMENT

Command: **test environment short/long r** (No.)

Long Tests (Dedicated SAT):

Note: Tests No. 126 and 127 are repeated for each carrier present in the cabinet. All calls associated with port carrier circuit packs are disrupted.

- Test No. 5 (Battery Charger Test)
- Test No. 126 (Carrier Power Unit Recycle Test)
- Test No. 127 (Carrier Power Unit Query)
- Test No. 124 (Emergency Transfer Query)
- Test No. 122 (Cabinet Query)
- Test No. 120 (Application Processor Query)

Short Tests:

Note: Test No. 127 is repeated for each carrier present in the cabinet.

- Test No. 5 (Battery Charger Test)
- Test No. 127 (Carrier Power Unit Query)
- Test No. 124 (Emergency Transfer Query)
- Test No. 122 (Cabinet Query)
- Test No. 120 (Application Processor Query)

Reset Commands

The reset command is used to reset the system and the Interface 2 circuit pack.

RESET SYSTEM COMMAND

The reset system commands are used to restart the system at an indicated level. The levels of recovery are defined under *System Initialization and Recovery* in this manual. No results for a reset command are displayed on the dedicated SAT or at INADS. The dedicated SAT is logged off.

Command: **reset system** "qualifier"

Qualifier: Level of recovery as specified below:

Qualifier	Recovery
1	Level 4
2	Level 3
3	Level 2
4	Level 1
5	See Note

Note: This level recovery is the same as a Level 1 recovery plus all 24-hour tests are run immediately.

The "reset system 1" command may disrupt in-progress calls. The "reset system 2, 3, 4, or 5" commands disrupt all calls in the system.

RESET INTERFACE COMMAND

This commands resets the Interface 2 circuit pack. When the AP is first administered or the Interface 2 circuit pack is replaced, the command must be entered. Test results for a "Test No. 117" are displayed as defined in this manual.

Note: This command interrupts operation of the AP.

Busyout Commands

The busyout commands are used to busyout the following maintenance objects:

- Port Circuit Packs (Boards)
- Port Circuit Pack (Ports)
- Voice Terminal Extensions (Stations)
- Trunks/Trunk Groups
- Data Channels
- Pooled Modems

Any of the above maintenance objects that are administered can be busied out, even those that are not installed. The result is that the maintenance object is placed in a maintenance busy state until it is released by the release command. This will prevent call processing software from using the busied out resource. In addition, a warning alarm is logged to indicate the busied out status.

The results of a busyout command are displayed on the SAT or at INADS. Figure 31 is an example of typical busyout command results. The following information is contained in the results:

- **Physical Location:** Physical location of the maintenance object—carrier, slot number, port number for ports and channel number for data channels

  Note: All port numbers busied out are listed.

- **Logical Name:** Logical name of the maintenance object
- **Result:** The results of the command for each port busied out—pass or fail
- **Error Code:** A system generated number that tells why a busyout command failed. Possible error codes are the "Common Error Codes" provided under *Error Codes* in this manual.

```
busyout port e0401

Port      Maintenance Name     Result     Error Code

E0401     ANA-LINE             PASS
```

Figure 31. Typical Busyout Command Results

A definition of the busyout commands according to maintenance object is provided in following order:

- Port Circuit Pack (Board)
- Port
- Voice Terminal Extension (Station)
- Trunk Group/Trunk
- Pooled Modem
- Data Channel

A listing of busyout commands according to maintenance object follows:

PORT CIRCUIT PACK

Command: **busyout board** "qualifier"

Qualifier: Circuit pack location for port circuit pack (b01, for example)

PORT

Command: **busyout port** "qualifier"

Qualifier: Location of port on port circuit pack (b0101, for example)

TRUNK/TRUNK GROUP

Command: **busyout trunk** "qualifier"

Qualifier: Trunk group number or trunk group number followed by a space and the member number. If the trunk group number is entered, all trunks in the group are busied out (maximum of four).

VOICE TERMINAL EXTENSION

Command: **busyout station** "qualifier"

Qualifier: Terminal extension number

POOLED MODEM

Command: **busyout modempool**

> ***Note:*** This command busyouts all administered Pooled Modems in the system. A specific Pooled Modem can be busied out using the "busyout board" command.

DATA CHANNEL

Command: **busyout datachannel** "qualifier"

Qualifier: Data channel number—(1 through 4)

Release Commands

The release commands are used to release the maintenance objects busied out by the busyout command. The results of a release command are displayed on the SAT or at INADS. If the maintenance object is not installed, "NO BOARD" is displayed. Otherwise, the results are the same as those for the busyout command discussed previously. The warning alarm generated by the busyout command is resolved.

Display Commands

The display command is used to display the Alarm Log, Error Log, current time, and initialization causes.

Command: **display alarms/errors/time/initcauses**

alarms: Alarm Log is displayed. The Alarm Log is described in the *System Maintenance* manual (555-200-105IS).

errors: Error Log is displayed (see *Error Log* in this manual.

time: Set Time Form is displayed (see Figure 32).

initcauses: Initialization Causes Form is displayed (see Figure 33). The Initialization Causes Form is described below.

The "Cause" statement on the Initializations Causes Form tells why the low-level maintenance software initiated the restart. The following "Cause" statements are possible:

Sanity time reset
Maint board reset
Power up reset
O/P request
Craft reboot request
Craft extended reboot request
NMI (memory) count request
BP count exceeded
SS count exceeded

Note: The last two statements listed indicate a bad CPU chip set in the Processor circuit pack.

The "Action" statement tells the action taken by the low-level maintenance software as a result of the "Cause." The following "Action" statements are possible:

Warm start performed
Level II cold start
Level I cold start
Reboot
Extended reboot
INADS called

```
display time                                                    Page 1 of 1

                                DATE AND TIME

DATE

      Day of the Week: Wednesday        Month: March
     Day of the Month: 21                Year: 1984

TIME

                  Hour: 13              Second: xx
                Minute: 51
```

Figure 32. Set Time Form

```
display initcauses

                                Initialization Causes

                    Cause                       Action

            Craft reboot request                Reboot
```

Figure 33. Typical Initialization Causes Form

List Configuration Commands

The list configuration commands are used to display various hardware and software configuration reports. The configuration reports are displayed on the SAT or at INADS.

HARDWARE CONFIGURATION REPORTS

Figure 34 is an example of a typical hardware configuration report. The following information is contained in the report:

- **Board Number:** Physical location of the circuit pack—carrier and slot number

  Note: This information does not apply to fixed position circuit packs. Only the carrier position is listed for these circuit packs.

- **Board Type:** Circuit pack name
- **Vintage:** Vintage of ROM on circuit pack (000000—065535 or "no board")

  Note: If the vintage is "no board" the board is administered but not physically installed.

- **Assigned Ports:** Port numbers of all administered ports on circuit pack (01—08)

The following command provides the hardware configuration reports:

Command: **list configuration** "qualifier"

Qualifier: The following qualifiers are allowed:

- all—all circuit packs installed are listed
- stations—all Analog Line, Hybrid Line, Digital Line and MET Line circuit packs installed are listed
- trunks—all CO Trunk, DID Trunk, Tie Trunk, and Auxiliary Trunk circuit packs installed are listed
- control—all fixed position circuit packs are listed
- board "xyy"—circuit pack installed in location xyy is listed (x = carrier and yy = slot number, b01 for example)

```
list configuration all                                          Page 1

Board
Number      Board Type          Vintage          Assigned Ports

xxx         xxxxxxxxxxxxxxx       xxxxxxxx       xx xx xx xx xx xx xx xx
A01         DIGITAL LINE          000021         01    03 04
A02         ANALOG LINE           000004            02 03 04
B03         CO TRUNK              000100         01 02 03 04 05 06 07 08
B04         TIE TRUNK             no board       01 02
E20         AUXILIARY TRUNK       000001
 C          MAINTENANCE           000005
 C          PROCESSOR             006913
 C          INTERFACE 1           000001
 C          MEMORY 1              000005
 C          MEMORY 2              no board
 C          MEMORY 3              no board
 C          TAPE CONTROL          000001
 C          NETWORK CONTROL       000001         01 02 03 04
 C          INTERFACE 2           000001
 C          INTERFACE 3           000001
 C          TONE/CLOCK            000004
 G          HCMR ROM              000774
 G          TRANSPORT             000012
 G          CONTROLLER            000013
 G          DATA/SERVO            000007
```

Figure 34. Partial Example of Display Output for "List Configuration All" Command

SOFTWARE CONFIGURATION REPORT

Figure 35 is an example of a typical software configuration report. The following relevant information is contained in the report:

- **Date of Update File:** Date and time that translations were last read from tape into memory.
- **Last tape backup of Translation Data:** Date and time that the last backup tape was made.

The following command provides the software configuration report:

Command: **list configuration software-vintage**

```
list configuration software-versions                    Page 1

                        SOFTWARE VERSIONS

                Date of Update File: 12:59 am  WED APR 20, 1983
              Update File old vintage: 000455
              Update File new vintage: 003376

           Memory-resident Software vintage: 003376
             Tape-resident Software vintage: 000455
        Last tape backup of Translation Data: 4:55 pm   TUE APR 19, 1983
```

Figure 35. Typical Software Configuration Report

Test Descriptions

The following is a numerical listing of the tests performed as the result of maintenance commands entered at a dedicated or remote SAT. A brief description is provided for each test.

- **Test No. 0 (Dial Tone Test)**

  In this test, the SPE sends a message to the on-board microprocessor to seize the port and checks that dial tone is returned.

- **Test No. 3 (Diagnostic Test)**

  The on-board microprocessor operates relays in the port circuit and checks for ground. If the trunk is loop start, it is set to ground start and returned to loop start after the test is completed.

- **Test No. 4 (Idle Time Slot Test)**

  This test removes time slots that are found bad (noisy when supposed to be idle) from service until the condition clears. Idle time slots are connected eight at a time to a general purpose tone detector. The general purpose tone detector checks for some non-idle samples on the eight time slots. The test runs through all time slots that are currently idle.

  When a group of eight time slots is not idle, the test isolates the faulty time slot by performing individual idle time slot tests on each of the eight. Any time slot that fails the retest is removed from service (subject to a maximum out of service level of 260).

  If any time slots are out of service, they are tested to see if they are still noisy, and restored to service if they are idle. After all time slots have been tested, all port circuit on-board microprocessors are short scanned to release any that are held reset.

- **Test No. 5 (Battery Charger Test)**

  The SPE sends a query message to the Maintenance circuit pack to check the battery charger for faults, rate of charge, presence of ac voltage, and low battery.

- **Test No. 6 (NPE Crosstalk Test)**

  This test verifies that the NPE assigned to the port/terminal only talks on the selected time slot, never crossing over to time slots reserved for other connections.

  In this test, three time slots are reserved: a random time slot and its one's complement on one bus (A or B), and another time slot on the other bus. The NPE is then made to talk on each selected time slot in turn. After each connection is made, an idle time slot test is run to checks all currently idle time slots to make sure that none are overwritten. If time slot(s) is corrupted, the talking is removed to verify that this particular NPE is the cause. If any time slots are still corrupted, they are removed from service.

- **Test No. 9 (NPE Crosstalk Test)**

  This test is basically the same as the analog terminal/port NPE crosstalk test (Test No. 6). The only difference is that the test is performed on both DCP channels. If this test fails on either channel, the terminal and DTDM are taken out of service.

- **Test No. 11 (EPF Restoral Test)**

  This test checks if the EPF in the port circuit can be successfully turned on. The SPE sends a message to on-board microprocessor to turn on the EPF and check if the EPF is in a overcurrent condition. This test is repeated once more five seconds later.

- **Test No. 13 (Voice and Control Channel Local Loop Test)**

  These tests check the information and control channels between the SPE and the Digital Line port circuit. The SPE sends a message to the on-board microprocessor to loop around both the information and control channels for the port. First, the I1 channel loop back test is run. The test is performed by sending a digital count from the Tone/Clock circuit pack on the I1 channel time slot and receiving the same digital count with a general purpose tone detector. The digital count looks like transparent data to the on-board microprocessor.

  While the I1 channel is still looped around, the S channel loop around test is performed. This test consists of sending four different transparent patterns to the on-board microprocessor, receiving them back and comparing them.

  The loop around test for the I2 (alternate) channel is then performed. This test is the same as the I1 channel loop around test and is performed only if a DTDM is administered.

  A conference test is done next for the I1 channel. This test is the same as the Analog Line terminal/port conference test.

- **Test No. 16 (Station Lamp Updates)**

  The SPE sends messages to the on-board microprocessor to light all lamps on the terminal as specified in translations. Each message contains information for four lamps.

- **Test No. 17 (Station Audits)**

  The SPE sends messages to the on-board microprocessor to perform switchhook, bad scan, and EPF inquiries, request ID, and update ringer (on or off).

- **Test No. 33 (Loop Around and Conference Test)**

  This test checks the port circuit hybrid and the NPE conference circuit.

- **Test No. 35 (Port Diagnostic Test)**

  The on-board microprocessor terminates the line and checks to see if a switchhook signal is present. If the signal is not present, the test fails. The test aborts if the terminal is busy.

- **Test No. 36 (Audit Update)**

  The SPE sends messages to the on-board microprocessor to detect if it can update the status of the switchhook, message lamp, administrative data (low/high gain), and ringer. The test aborts if the terminal is busy.

- **Test No. 40 (Tone Generator Transmission Test)**

  The SPE sends a message to the on-board microprocessor for the tone generator to generate the touch-tone digits one at a time. The digits are received and checked by a Tone Detector touch-tone detector. If any of the digits fail, the test is repeated using a touch-tone detector in another Tone Detector.

  For the second part of the test, the SPE sends a message to the on-board microprocessor for the tone generator to generate call progress tones that are assigned to dedicated time slots. A Tone Detector general purpose tone detector listens for the tones and measures the value, mode, and loss for each tone.

  For the last part of the test, the SPE next sends a message to the on-board microprocessor for the tone generator to generate tones that are not assigned a dedicated time slot. A Tone Detector general purpose tone detector listens for the tones and measures the value, mode, and loss for each tone. If any of the measured values are not within limits, the test is repeated using a general purpose tone detector in another Tone Detector.

- **Test No. 41 (Tone Generator Audit/Update)**

  The SPE sends messages to the on-board microprocessor to check the DSP sanity, verify that the tone generator can switch tones from one bus to another bus, and update all time slot values.

- **Test No. 42 (Tone Detection Test)**

  The SPE sends a message to the on-board microprocessor to cause a general purpose tone detector to listen for specific system access tones. The on-board microprocessor sends a message indicating the detected value of each tone.

- **Test No. 43 (Tone Detector Audit/Update)**

  This test consists of a DSP self test, a DSP sanity test, and a general purpose tone detector update test.

- **Test No. 47 (Hybrid and Conference Test)**

  This test uses a 1004-Hz tone at -16 dBm and 0 dBm provided by the Tone/Clock circuit pack to test the hybrid circuit and conference circuit associated with the port/terminal. It also tests some of the per NPE channel gain and sample registers.

  The hybrid tests consists of a two reflective and one non-reflective test. The two reflective tests use the low level tone. The first reflective test uses high NPE gain and a short loop (600-ohm) balancing impedance (R). The second reflective test uses low NPE gain and a long loop (resistive/capacitive network) balancing impedance (RC). The on-board microprocessor puts the port in the loop-around mode and a general purpose tone detector measures the losses for the two tests.

  The reflective test uses the high level tone, low NPE gain, and a 600-ohm termination. The on-board microprocessor terminates the port and a general purpose tone detector measures the loss for the test.

  The conference test checks the operation of the NPE conference circuit associated with the port/terminal. Four tests are run using different NPE gains and input signal levels. Each test conferences six signals. The general purpose tone detector measures the looped around output for notched noise level.

- **Test No. 48 (Ringing Application Test)**

  The on-board microprocessor applies a low-current ringing voltage to the line to see if the voice terminal is present. If the terminal is not present, the test fails. The test aborts if the terminal is busy.

- **Test No. 50 (NPE Audit)**

  The SPE sends a message to the on-board microprocessor to update the NPE translation for all NPEs on the circuit pack with translated ports. The on-board microprocessor updates the NPE memory, reads the memory to confirm the data just written, and reports errors.

- **Test No. 51 (Ringing Application Test)**

  This test checks the ringing application circuitry common to all ports on an Analog Line circuit pack.

- **Test No. 52 (Control Channel Loop Around Test)**

  This test checks the operation of the SAKI, on-board microprocessor, and bus A buffers. The SPE sends circuit pack code inquiry and circuit pack vintage requests to the on-board microprocessor and checks the replies.

- **Test No. 53 (SAKI Reset Test)**

  This test verifies the SAKI sanity mechanism is operational. The SPE sends a message to cause the on-board microprocessor to reset and release. If the on-board microprocessor cannot be reset or released from the reset condition, the test fails.

- **Test No. 56 (EPF Restoral Test)**

  This test checks if the EPF in the port circuit can be successfully turned on. The SPE sends a message to on-board microprocessor to turn on the EPF and check if the EPF is in a overcurrent condition.

- **Test No. 57 (Hybrid Circuit and Conference Test)**

  This test checks the amount of reflection from the hybrid loop around circuitry and does a conference test. The Tone/Clock circuit pack places a 1004-Hz tone on a time slot that the port circuit is listening on. A general purpose tone detector is connected to another time slot that the same port circuit is talking on. The on-board microprocessor places the port in the loop around mode and the general purpose tone detector measures the level of the reflected signal.

  The conference test is performed after the hybrid test. The conference test is the same as the analog terminal/port conference test.

- **Test No. 58 (Digital Loop Around Test)**

  This test checks the control channel between the SPE and the port's digital circuitry. The SPE sends transparent data to the on-board microprocessor and compares the data echoed back. This test is repeated three times.

- **Test No. 59 (Remote Station Test)**

  This test checks the digital control pair form the port circuit to the terminal. The on-board microprocessor sends a message to the terminal and checks for a proper return message. This test is repeated three times.

- **Test No. 60 (Station Lamp Updates)**

  The SPE sends a message to the on-board microprocessor to light all lamps on the terminal as specified in translations.

- **Test No. 61 (Station Audits)**

  The SPE sends messages to the on-board microprocessor to perform a switchhook, bad scan, and EPF inquiry. The test aborts if the terminal is busy.

- **Test No. 62 (Ringer Update)**

  The SPE sends a message to the on-board microprocessor to cause the terminal ringer to alert and turn off.

- **Test No. 64 (HCMR Read Test)**

  The SPE reads all the data blocks on the tape and flags the bad blocks if errors are found. This test takes 10 to 15 minutes to run.

- **Test No. 65 (HCMR Read/Write Test)**

  The SPE reads and writes to the unused portion space on the tape to exercise the Transport circuit pack.

- **Test No. 66 (HCMR Diagnostic Test)**

  This test checks the ROM and RAM as well as many other devices in the Controller circuit pack. The motor is operated and checked. Data is written in a maintenance block and read.

- **Test No. 67 (HCMR Buffer Test)**

  This test checks the shared RAM in the Controller circuit pack.

- **Test No. 68 (HCMR Loopback Test)**

  This test operates latches in the Tape Control circuit pack to check if the Tape Control circuit pack can send and receive the correct data.

- **Test No. 69 (HCMR Status Test)**

  The SPE requests the Controller circuit pack to write its current status into the two status words in its RAM buffer. In the normal read/write operation, these words are always passed to the maintenance software whenever the Tape Transport circuit pack issues an error report via the Controller circuit pack. In the idle mode, this test is always running in the background.

- **Test No. 73 (Electronic Power Feed Test)**

  This test consists of an "E" lead and "M" lead test. The "E" lead test checks for proper activation and deactivation of the port's "E" lead. The "M" lead test checks the "M" lead electronic power feed current flow. The SPE sends an "M" lead test request to the on-board microprocessor and receives the results. The returned results are measured to see if there is a port or external tie trunk line failure.

- **Test No. 77 (Software Initiation Interrupt)**

  This test checks the three software initiated interrupts can be activated.

- **Test No. 78 (Memory Management On/Off)**

  This checks that the 16 segment descriptors in the memory management circuit can be loaded and accessed properly.

- **Test No. 79 (Overflow Stack)**

  This test checks that the stack overflow RAM (part of the on-board memory) can serve as the overflow stack for any process stack operation.

- **Test No. 80 (ROM Checksum)**

  This test checks if the monitor program stored in the on-board ROM has been corrupted or not.

- **Test No. 82 (Non-Maskable Interrupt Test)**

  This test causes all kinds of NMIs that are generated by the Processor circuit pack to occur. NMIs that are not generated by the Processor circuit pack are not tested.

- **Test No. 83 (Sanity Timer)**

  This test causes the sanity timer to time out and see whether the SPE will be reset.

- **Test No. 85 (Memory Read All Test)**

  Every word in Memory is read. If there are any transient single bit errors, they are corrected. If there are any faults in the memory, an interrupt is generated and the test fails.

- **Test No. 86 (RAM Checksum)**

  This test verifies that the test and prototype data in RAM are not corrupted.

- **Test No. 87 (Memory Error Detection)**

  This test verifies that the Memory error detection, error correction, and error exception circuitry is functioning.

- **Test No. 90 (Tone Generator Crosstalk Test)**

  In this test, the tone generator places dial tone on time slot X and the Tone Detector listens on eight idle time slots, one at a time, for tone. The test is repeated on the complement of time slot X.

- **Test No. 92 (8-Bit On-Board Microprocessor A Loop Around Test)**

  The SPE sends special loop around messages to check the dual-port RAM. The messages are intercepted by the on-board microprocessor A and sent back with no other action taken. If the entire sequence of messages is successfully returned to the SPE, the test passes.

- **Test No. 93 (8-Bit On-Board Microprocessor A Reset Test)**

  This test checks the ROM program store, internal and external RAM, and the bus between the microprocessor and the SAKI. It also verifies the functionality of the SAKI registers.

- **Test No. 94 (Control Channel Integrity Test)**

  This test checks that the SPE can update the control channel. The SPE sends circuit pack and vintage requests and checks for a response.

- **Test No. 95 (Time-of-Day Clock Test)**

  This test consists of two checks of the time-of-day clock chip. The first check determines the deviation of the clock from the reference counter on the SPE. If the deviation is greater than ten seconds the test fails. The second check tests the accuracy of the clock for short intervals.

- **Test No. 96 (Modem NPE Crosstalk Test)**

  The test is basically the same as the analog terminal/port NPE crosstalk test (Test No. 6). The only difference is that the test is repeated on both ports of the conversion resource.

- **Test No. 97 (Modem Conference Test)**

  This test checks the conference circuit on the analog port of the conversion resource. The test uses a 1004-Hz tone at -16 dBm and 0 dBm provided by the Tone/Clock circuit pack.

- **Test No. 98 (Conversion Resource Loop Around Test)**

  The SPE sets up time slot connections that cause a Network Control data channel to be connected to the digital port of a conversion resource and the analog port to be connected to itself. The Network Control data channel sends bit streams to the digital port and monitors for their reception. The data channel checks the bit streams for errors.

- **Test No. 99 (Modem Audits)**

  The SPE sends messages to the on-board microprocessor to see if it can update the status information for both ports of the conversion resource.

- **Test No. 101 (Reset Test)**

  This test puts the Maintenance circuit pack is put to sleep and then reset, which in turn invokes initiation tests. All drivers are reset during this test. The dedicated SAT is logged off.

- **Test No. 102 (Outpulse Relay Test)**

  This test detects loop current on the line from the modem. This test validates the INADS trunk connection.

- **Test No. 103 (Analog Loop Test)**

  This test unbalances the hybrid and tries to send data.

- **Test No. 104 (Dual-Port RAM Test)**

  This is a coordinated test of the dual-port RAM.

- **Test No. 106 (Sanity Handshake)**

  The SPE sends a message to the Maintenance circuit pack and expects a reply message. If a timeout occurs before receiving a reply, the test fails.

- **Test No. 107 (Data Channel Reset)**

  This test resets and restarts the whole data channel. All existing calls are dropped.

- **Test No. 108 (Dual-Port RAM Test)**

  This test checks the integrity of the control dual-port RAM by using the combination of local loopback and a partial dual-port RAM test.

- **Test No. 109 (Maintenance Loop Around Test)**

  The SPE places a call from one data channel to another data channel. The SPE then talks on one channel while listening to the other channel and compares the results.

- **Test No. 110 (Data Channel Crosstalk Test)**

  This test is very similar to Test No. 109 except the call is placed on a specific time slot. After call is set up, a NPE crosstalk test (Test No. 6) is performed.

- **Test No. 111 (Data Channel Local Loopback Test)**

  This test is identical to Test No. 108 except a different command is issued by the SPE.

- **Test No. 114 (Diagnostic Test—Auxiliary Trunk)**

  The SPE sends a message to the on-board microprocessor to operate a relay in the port circuit. If ground is detected, the test passes.

- **Test No. 116 (Interface 2 Handshake)**

  The SPE sends a handshake message to the software package running on Interface 2 and expects a correct reply within one second.

- **Test No. 118 (Interface 2 Read Status)**

  The SPE sets two words in the Interface 2 memory space, the first to a set value and the second to zero. The SPE waits for one second and reads the memory element and

checks it against zero. If it is zero, the handshake fails. If the new value of the second memory element is the value that was written to the first memory element plus one, the test has completed successfully.

- **Test No. 119 (S Bus Check)**

  The SPE reads a few selected words in the Interface 2 memory space across the S bus to check the link.

- **Test No. 120 (Applications Processor Query)**

  The SPE sends a message to the Maintenance circuit pack to check the status of alarms for the Applications Processor.

- **Test No. 122 (Cabinet Query)**

  The SPE sends a message to the Maintenance circuit pack to check if the fans are on and if there is a over temperature alarm active.

- **Test No. 124 (Emergency Transfer Query)**

  The SPE sends a message to the Maintenance circuit pack to check the state of the emergency transfer control switch.

- **Test No. 126 (Carrier Power Unit Recycle Test)**

  The SPE sends a message to the Maintenance circuit pack to turn off the carrier power units for one second and then turn the power units back on. After one second, the power units are checked for active alarms. If alarms are active, the SPE sends a message to turn the fault power unit off.

- **Test No. 127 (Carrier Power Unit Query)**

  The SPE sends a message to check if the power units are active or non-active.

Error Codes

The following is a list of error codes and description according to "Test No." The list is preceded by error codes common to all tests. These error codes also apply to the reset and busyout maintenance commands. This list of error codes is not complete and will be expanded in the final issue of this manual.

Common Error Codes

Fail

None.

Abort

Code	Description.
100	Test could not be completed at this time.
1000	Port is busy.
1001	CM couldn't seize port.
1002	No more time slots.
1003	No more time receivers.
1004	Port seized during testing.
1005	Test inapplicable to present configuration.
1006	Port is out of service.
1007	Port not translated.
1008	No more ringing circuits on circuit pack.
1009	Pass with considerations (see particular Test No.)
1010	Port is busied out.
1011	Port is in service.
2000	Uplink message timeout.
2001	Time-of-day clock hardware error.
2002	Test encountered inline faults.
62525	No room in Image table.
62526	No room in reply path table.
62527	No room in message queue.

Test 0: Dial Tone Test

Abort

None.

Fail

Code	Description.
2002	Seizure portion of test failed due to hardware problem. Fault is usually caused by a disconnected trunk.

Pass

Code	Description.
1009	Detected tone was not pure dial tone.

Test 3: CO Trunk Diagnostic Test

Abort

None.

Fail

None.

Test 4: Idle Time Slot Test

Fail

Code	Description.
X	X bad time slots were detected.

Abort

None.

Test 5: Battery Charger Test

Fail

Code	Description.
8	Battery reserve fault.
4	High charging rate.
2	Low Battery voltage.
1	No ac power.

Abort

None.

Test 6: NPE Crosstalk Test

Fail

Code	Description.
X	X time slots taken out of service.

Abort

None.

Test 9: Digital Line NPE Crosstalk Test

Fail

Code	Description.
1	Channel 1 (Digital Line, PDM, Trunk Data Module) NPE crosstalk test.
2	Channel 2 (DTDM) NPE crosstalk test.

Abort

Code	Description.
1	Channel 1 NPE crosstalk test.
2	Channel 2 NPE crosstalk test.

Test 11: Digital Line EPF Restoral Test

Fail

Can never fail.

Abort

Code	Description.
Blank	Could not send message downlink.

Test 13: Digital Voice and Control Local Loop Test

Fail

Code	Description.
14	Primary Voice Channel test failed (greater than 5 errors).
15	Control Channel test failed (one of the four patterns did not match).
16	Secondary Channel test failed.
7	Conference test failed (either on primary or secondary channel).

Abort

Code	Description.
Blank	Could not send message to loop around port.
Blank	Could not send transparent message for control channel loop.
14	Timed out on response from primary voice channel test.
15	Timed out on response from control channel loop test.
16	Secondary channel test timed out.

Test 16: Digital Line Station Lamp Updates

Fail

Can never fail.

Abort

Code	Description.
Blank	Could not use timer driver for waiting between updates.

Blank	Problem in waiting loop.
1,3	Lamp update did not go through successfully (possible link problem).

Test 17: Digital Line Station Audits

Fail

Can never fail (but check the Error Log for logged errors).

Abort

Code	Description.
Blank	Software data error.
1	Switchhook audit timed out.
2	ID request fails, health bit is bad, or no response from on-board microprocessor.
3	No response from EPF audit.
4	Bad scan audit timed out.
5	Ringer update aborted (station in "ready-for-service" or "out-of-service" state).

Test 33: Loop Around and Conference Test

Fail

Code	Description.
1	Non-reflective 404-Hz tone.
2	Non-reflective 1004-Hz high gain tone.
3	Non-reflective 1004-Hz low gain tone.
4	Non-reflective 2804-Hz tone.
7	Conference test.
129	Reflective 404-Hz tone.
130	Reflective 1004-Hz high gain tone.
131	Reflective 1004-Hz low gain tone.
133	Reflective 2804-Hz tone.

Abort

Same as above.

Test 35: Port Diagnostic Test

Abort

None.

Fail

None.

Test 36: Audit Update

Fail

Code	Description.
1	Switchhook audit.
5	Lamp update.
7	Translation update.
8	Ringer update.

Abort

None.

Test 40: Tone Generator Transmission Test

Fail

Code	Description.
1	Touch-tone generation failed.
101	Generation of dial tone failed.
102	Generation of ringback failed.
103	Generation of busy tone failed.
104	Generation of reorder failed.
105	Generation of 440 Hz failed.
106	Generation of recall dial tone failed.
107	Generation of confirmation tone failed.
108	Generation of intercept failed.

110	Generation of 2225-Hz level invalid.
111	Generation of 404-Hz level invalid.
112	Generation of 1004-Hz low level invalid.
113	Generation of 1004-Hz high level invalid.
114	Generation of 2804-Hz level invalid.
115	Generation of digital milliwatt level invalid.
116	Generation of count sequence invalid.
121	Generation of quiet tone failed.

Abort

None.

Test 41: Tone Generator Audit/Update

No additional data returned.

Test 42: Tone Detection Test

Fail

Code	Description.
1	Touch-tone detection failed.
2	Digit blocking failed.
3	Speech passing failed.
101	Detection of dial tone failed.
102	Detection of ringback failed.
103	Detection of busy tone failed.
104	Detection of reorder failed.
105	Detection of 440 Hz failed.
106	Detection of recall dial tone failed.
107	Detection of confirmation tone failed.
108	Detection of intercept failed.
109	Detection 770 Hz as a call progress tone.
110	Detection of 2225 Hz invalid.
111	Detection of 404-Hz low level invalid.
112	Detection of 404-Hz high level invalid.
113	Detection of 1004-Hz low level invalid.
114	Detection of 1004-Hz high level invalid.
115	Detection of 2804-Hz level invalid.
116	Detection of digital milliwatt level invalid.
117	Detection of data count sequence invalid.
118	Detection of voice count sequence failed.
119	Detected idle on a busy time slot.
120	Detected noise on 1004-Hz tone.
121	Detection of quiet tone failed.

Abort

None.

Test 43: Tone Detector Audit/Update

No additional data returned.

Test 47: Analog Line Hybrid and Conference Test

Fail

Code	Description.
19	Reflective 1004-Hz tone (gain=low, balance=R).
21	Reflective 1004-Hz tone (gain=high, balance=RC).
22	Non-reflective 1004-Hz tone (gain=low, balance=R).

7	Conference test.

Abort

None.

Test 48: Analog Line Ringing Application Test

Abort

None.

Fail

None.

Test 50: NPE Audit

No additional data returned.

Test 51: Ringing Application Circuit Test

No additional data returned.

Test 52: Control Channel Loop Around Test

No additional data returned.

Test 53: SAKI Reset Test

Fail

Code	Description.
1	On-board microprocessor failed to be reset.
2	On-board microprocessor failed to be restarted.

Abort

None.

Test 56: Hybrid Line EPF Restoral Test

Fail

None.

Abort

Code	Description.
Blank	Could not send message downlink.

Test 57: Hybrid Line Hybrid Circuit and Conference Tests

Fail

Code	Description.
57	Hybrid circuit test.
7	Conference test.

Abort

Code	Description.
57	Hybrid circuit test.
7	Conference test.

Test 58: Hybrid Line Digital Loop Around

Fail

Code	Description.
1	Loop back failed on first pattern.
2	Loop back failed on second pattern.
3	Loop back failed on third pattern.

Abort

Code	Description.
1	Aborted on first pattern.
2	Aborted on second pattern.
3	Aborted on third pattern.
8	Could not send loop message downlink.

Test 59: Hybrid Line Remote Station Test

Fail

Code	Description.
1	Failed on first try.
2	Failed on second try.
3	Failed on third try.

Abort

Code	Description.
3	Unsuccessful attempt—test did not run.

Test 60: Hybrid Line Station Lamp Updates

Fail

Can never fail.

Abort

Code	Description.
1	Timer problem.
2	Wait loop problem.
3	Lamp updates not done because station is out-of-service or in ready-for-service state.

Test 61: Hybrid Line Station Audits

Fail

Can never fail (but check the Error Log for logged errors).

Abort

Code	Description.
Blank	Software data error or audit disallowed because of link state.
1	Switchhook audit—no response.
2	Bad scan—no response.
3	EPF audit received no response or bad response.

Test 62: Hybrid Line Ringer Update

Fail

Can never fail.

Abort

Code	Description.
3	Unsuccessful update (possible link problem).

Test 64: HCMR Read Test

Fail or Abort

Code	Description.
1	Cartridge not in place.
513	Tape/Control circuit pack malfunction.
769	I/O buffer failed.
1537	Tape hardware error.
1793	Tape error.
2049	Tape hardware error due to read/write.
2305	Tape error due to read/write.
2561	Bad block.
9000	Bad data move path.
9001	Bad block number.
9002	Bad file type.
9003	Bad byte count.
9004	Bad operation code.
9005	System call error.
9006	Failure on read.
9007	Failure on write.
9008	New tape.
9009	Operation timed out.
9010	Tape OPEN failed.
9011	Read failed on primary file, backup used.

9012	Tape already opened.
9013	Tape ID has changed.
9014	Error on tape close.
9015	Tape maintenance test failed.
9016	Not enough room on tape.
9017	No hardware reset.
9018	No hardware present.

Test 65: HCMR Read/Write Test

Fail or Abort

See Test No. 64.

Test 66: HCMR Diagnostic Test

Fail or Abort

See Test No. 64.

Test 67: HCMR Buffer Test

Fail or Abort

See Test No. 64.

Test 68: HCMR Loopback Test

Fail or Abort

See Test No. 64.

Test 69: HCMR Status Test

Fail or Abort

See Test No. 64.

Test 73: Tie Trunk Seizure Test

Fail

None.

Abort

None.

Test 74: Tie Trunk EPF Test

Fail

Code	Description.
1	E-lead test.
2	M-lead test.

Abort

Same as for *Fail.*

Test 77: Processor Software Initiation Interrupt

Fail

None.

Abort

None.

Test 78: Processor Memory Management On/Off

Fail

None.

Abort

None.

Test 79: Processor Overflow Stack

Fail

None.

Abort

None.

Test 80: Processor ROM Checksum

Fail

None.

Abort

None.

Test 82: Processor NMI Test

Fail

None.

Abort

None.

Test 83: Processor Sanity Timer

Fail

None.

Abort

Code	Description.
1	Timer manager error.

Test 85: Memory Read All Test

Fail

None.

Abort

None.

Test 86: Memory RAM Checksum

Fail

None.

Abort

None.

Test 87: Memory Error Detection

Fail

None.

Abort

None.

Test 90: Tone Generator Crosstalk Test

No additional data returned.

Test 92: Network Control 8-Bit On-Board Microprocessor A Loop Around Test

Fail

Code	Description.
X	Loop around aborted Y times and failed X times.

Abort

None.

Test 93: Network Control 8-Bit On-Board Microprocessor A Reset Test

No additional data returned.

Test 94: Control Channel Integrity Test

Fail

Code	Description.
X	Communication was successful with X out of 3 on-board microprocessors.

Abort

None.

Test 95: Time-of-Day Clock Test

Pass or Fail

Code	Description.
X	X seconds elapsed on time-of-day clock during a 10 second interval.

Abort

None.

Test 96: Modem NPE Crosstalk Test

Fail

None.

Abort

Code	Description.
6000	Resources busy.
6001	Resources busy.

Test 97: Modem Conference Test

Fail

None.

Abort

Code	Description.
4000	Resources busy.

Test 98: Conversion Resource Loop Around Test

Fail or Abort

Code	Description.
5000:	Cannot allocate digital port of the conversion resource for testing.
5001:	Cannot open data channel 3 for testing.
5002:	Cannot reserve the data channel for testing.
5003:	Cm_orig failed.
5004:	Cannot allocate analog port of the conversion resource for testing.
5005:	Cm_orig failed.
5006:	Maintenance activate the conversion resource failed.
5007:	Data channel off hook failed.
5008:	Handshake between the data channel and the digital port failed.
5009:	Handshake between the data channel and the digital port failed.
5010:	Data loop around failed.
5011:	Cm_pt_disc failed.
5012:	Cm_pt_disc failed.
5013:	Loss of carrier disconnect test failed.

Test 99: Modem Audits

Fail

None.

Abort

None.

Test 101: Maintenance Circuit Pack Reset

Fail

Code	Description.
10104	Driver could initiate wake-up.
10105	Driver failed wake-up.
10106	Maintenance circuit pack still asleep after wake-up.

Abort

Code	Description.
10101	Can_mb flag in pdfile cancels this test.
10102	Could not gain exclusive access to COM.
10103	Could not put Maintenance circuit pack to sleep.

Test 102: Maintenance Circuit Pack Outpulse Relay Test

Fail

Code	Description.
10204	Maintenance circuit pack reported test failure.

Abort

Code	Description.
10201	Could not get exclusive access to COM.
10202	Could not send test message.
10203	Maintenance circuit pack did not respond to test request.

Test 103: Maintenance Circuit Pack Analog Loop Test

Fail

Code	Description.
10304	Maintenance circuit pack reported test failure.

Abort

Code	Description.
10301	Could not get exclusive access to COM.
10302	Could not send test message.
10303	Maintenance circuit pack did not respond to test request.

Test 104: Maintenance Circuit Pack Dual-Port RAM Test

Fail

Code	Description.
10403	Driver did not respond to test request.
10404	Driver reported test failure.

Abort

Code	Description.
10401	Could not get exclusive access to COM.
10402	Could not send driver test request.

Test 106: Maintenance Circuit Pack Sanity Reset

Fail

Code	Description.
10603	Maintenance circuit pack did not respond to handshake.

Abort

Code	Description.
10601	Could not get exclusive access to COM.
10602	Could not send Maintenance circuit pack test request.

Test 107: Network Control Data Channel Reset

Test 108: Network Control Dual-Port RAM Test

Fail

Code	Description.
769	Control dual-port RAM failure.

Abort

None.

Test 109: Network Control Loop Around Test

Fail

Code	Description.
10940	Failed talk test.
10941	Failed listen test.
10970	"Receive" kernel call failed.
10972	Bad response from auxiliary port.
10973	Bad response from data channel.
10974	Timeout waiting for call arrival.
10975	Unknown message received during test.

Abort

Code	Description.
10900	Maintenance test disabled.
10901	Could not allocate resource (port busy?)
10902	Could not gain exclusive access to COM.
10903	Could not open data channel.
10904	Could not place a notification path.
10915	Could not read translation data.
10916	Could not find extension of data channel.
10920	Could not place a call to data channel.
10971	No auxiliary port to test with.

Test 110: Network Control Data Channel Crosstalk Test

Fail

Code	Description.
11012	Could not get a timeslot.
11013	Could not enter loopback mode.
11014	Could not send ringing stimulus.
11015	Time out waiting for off-hook.
11016	Could not get ringer-off stimulus.
11040	Failed talk test.
11070	"Receive" kernel call failed.
11073	Bad response from data channel.
11074	Time out waiting for call arrival.
11075	Unknown message received during test.

Abort

Code	Description.
11000	Maintenance test disabled.
11001	Could not allocate resource (port busy?).
11002	Could not gain exclusive access to COM.
11003	Could not open data channel.
11004	Could not place a notification path.

Test 111: Network Control Data Channel Local Loopback Test

Fail

Code	Description.
11120	Could not put data channel in callback mode.
11140	Failed talk test.
11170	"Receive" kernel call failed.
11173	Bad response from data channel.
11174	Time out waiting for call arrival.
11175	Unknown message received during test.

Abort

Code	Description.
11100	Maintenance test disabled.
11101	Could not allocate resource (port busy?).
11102	Could not gain exclusive access to COM.
11103	Could not open data channel.
11104	Could not place a notification path.

Test 114: Auxiliary Trunk Diagnostic Test

Fail

None.

Abort

None.

Test 115: Interface 2 Alarm

Fail

Never.

Abort

Never.

Test 116: Interface 2 Handshake

Fail

Code	Description.
1	No Interface 2 circuit pack located in carrier.
6	No reply received from Interface 2 to message handshake.
7	Reply received from Interface 2 but data does not checkout.
12	Timer expires before channel.

Abort

Code	Description.
2	Open channel to send handshake message fails. May be in use by some other process.
3	Send of handshake message failed.
4	Cannot set alarm for wait on handshake reply.
5	Receive of message from timer/Interface 2 failed.
8	Handshake message received was of wrong class.
9	Set timer for wait on channel failed.
10	Cannot get channel to Interface 2. May be in use by some other process.
11	Partial path to sb_con destroyed, cannot get channel to Interface 2.
13	Bad receive, did not get requested class message.

Test 117: Interface 2 Start

Fail

Code	Description.
2	Interface 2 could not be reset.
101	Sanity call to Interface 2 fails.
102	Sanity check of Interface 2 fails (boot program not running).
103	Read from tape fails.
104	Write to Interface 2 memory fails.
105	Start of Interface 2 after successful download fails.

Abort

Code	Description.
3	Cannot get path to the tape controller.
4	Cannot open tape (someone else is using it).
5	Create data move path, from tape_on to map process' fails.

Test 118: Interface 2 Read Status

Fail

Code	Description.
1	No Interface 2 circuit pack located in carrier.
6	Interface 2 does not properly respond to test data given to it.

Abort

Code	Description.
2	Write to Interface 2 memory fails.
3	Cannot set wait timer.
4	Receive of wait timer message fails.
5	S bus read from Interface 2 memory fails.

Test 119: S Bus Check

Fail

None.

Abort

Never.

Test 120: AP Query

Fail

None.

Abort

Code	Description.
1	Could not get path to SPE.
2	Could not send message to Maintenance circuit pack.
3	Could not receive message from Maintenance circuit pack.

Test 122: Cabinet Query

Fail

Code	Description.
1	Over temperature in the cabinet.
2	Air flow alarm is raised.

Abort

1	Could not get path to SPE.
2	Could not send message to Maintenance circuit pack.
3	Could not receive message from Maintenance circuit pack.

Test 124: Emergency Transfer Query

Fail

Code	Description.
1	Manual off.
2	Manual on.

Abort

1	Could not get path to SPE.
2	Could not send message to Maintenance circuit pack.
3	Could not receive message from Maintenance circuit pack.

Test 126: Carrier Power Unit Recycle Test

Fail

None.

Abort

None.

Test 127: Carrier Power Unit Query

Fail

None.

Abort

1	Could not get path to SPE.
2	Could not send message to Maintenance circuit pack.
3	Could not receive message from Maintenance circuit pack.

FACILITIES ACCESS TEST

The facilities access test provides a voice terminal user the capability of making test calls to access specific trunks, touch-tone receivers, time slots, and system tones. The test call can be made by a local voice terminal user by dialing an access code (197 is the initial default value) or by an INADS terminal user over a trunk. The current access code can be obtained by displaying the Features Access Code form.

The following call descriptions are for local calls. If the calls are made from INADS, the access code must be preceded by the remote access telephone access number.

TRUNK TEST CALL

The trunk test call accesses specific Tie or CO trunks. DID trunks cannot be accessed.

To make the call:

1. Dial the facilities access test code and listen for dial tone.
2. Dial the 5-digit port number "xyyzz"

   x = Carrier number (A=1, B=2, C=3, D=4, E=5)

   yy = Slot number (01—20)

   zz = Port number (01—08)
3. Listen for one of the following tones:
   - Dial Tone—trunk is connected. Go to Step 4.
   - Reorder Tone—trunk is busy or maintenance busy
   - Intercept Tone—this is not a trunk or touch-tone receiver
4. Make call.

TOUCH-TONE RECEIVER TEST CALL

The touch-tone receiver call accesses and tests the four touch-tone receivers located on the Tone Detector circuit pack. The INADS voice terminal must be a touch-tone model.

To make the call:

1. Dial the facilities access test code and listen for dial tone.
2. Dial the 5-digit port number "xyyzz".

   x = Carrier number (A=1, B=2, C=3, D=4, E=5)

   yy = Slot number (01—20)

   zz = Touch-Tone Receiver Port number (01, 02, 05, or 06)
3. Listen for one of the following tones:
   - Dial Tone—touch-tone receiver is connected. Go to Step 4.

- Reorder Tone—touch-tone receiver is busy or maintenance busy
- Intercept Tone—this is not touch-tone receiver or trunk

4. Dial **1234567890*#** and listen for dial tone (test passed) or intercept tone (test failed).

   Note: The test fails if the touch-tone receiver cannot recognize all of the touch-tone signals.

TIME SLOT TEST CALL

The time slot test call connects the voice terminal user to a specific time slot located on the TDM buses (A or B) or out-off-service time slots.

Specific Time Slots

To make the call:

1. Dial the facilities access test code and listen for dial tone.
2. Dial the 3-digit time slot number "xxx" (see below).

   xxx = Time slot number (000—255 on bus A and 256—511 on bus B)

3. Listen for one of the following tones:
   - Confirmation Tone—time slot is idle or maintenance busy
   - Reorder Tone—time slot is busy
   - Dedicated Tone—tone on time slot (see Table A)

Out-of-Service Time Slots

To make the call:

1. Dial the facilities access test code and listen for dial tone.
2. Dial ** and listen for the following tones:
   - Confirmation Tone—connection is made. Go to Step 3.
   - Reorder Tone—no time slots are out-of-service
3. Repeat from Step 1 to alternate between out-of-service time slots on TDM bus A and B.

SYSTEM TONE TEST CALL

The system tone test call connects the voice terminal user to a specific system tone.

To make the call:

1. Dial the facilities access test code and listen for dial tone.
2. Dial * followed by the two-digit tone identification number (see Table D).
3. Listen for tone as listed in Table D.

TABLE D. System Access Tones—Facilities Access Test

Two-Digit Code	Tone
00	Null Tone
01	Dial Tone
02	Reorder Tone
03	Intercept Tone
04	Busy Tone
05	Recall Dial Tone
06	Confirmation Tone
07	Calls Waiting Tone
08	Alerting Tone
09	Special Audible Alerting Tone
11	697 Hz*
12	770 Hz*
13	852 Hz*
14	941 Hz*
15	1209 Hz*
16	1336 Hz*
17	1447 Hz*
18	1637 Hz*
19	Dial Tone
20	Chime

*These tones are used to generate touch-tone signals.

TABLE D. System Access Tones—Facilities Access Test (Contd)

Two-Digit Code	Tone
21	350 Hz
22	440 Hz
23	480 Hz
24	620 Hz
25	2025 Hz
26	2225 Hz
27	Counter
28	Calls Waiting 2
29	Calls Waiting 3
30	Busy Verification
31	Executive Override
32	Incoming Call Identification
33	Dial Zero
34	Attendant Transfer
35	Test Calls
36	Recall on Don't Answer
37	Alerting
38	Camp-On Recall
39	Camp-On Confirmation
40	Hold Recall
41	Hold Confirmation
42	Zip Tone
43	2804 Hz
44	1004 Hz (-16 db)
45	1004 Hz (0 db)
46	404 Hz
47	105-Type Test Line, Default Sequence
48	Redirect Tone
49	Voice Signaling Tone
50	Digital Milliwatt
51	440 Hz + 480 Hz (Audible Alerting)
52	Music
53	100-Type Test Line
54	102-Type Test Line

ABBREVIATIONS AND ACRONYMS

A

ALU	Arithmetic and Logic Unit
AP	Applications Processor
AP/A	Applications Processor/Adjunct
Aux	Auxiliary

C

CCMS	Control Channel Message Set
CDDR	Call Detail Recording and Reporting
CO	Central Office
Codec	Coder/Decoder
CPE	Client-Provided Equipment
CPTR	Call Progress Tone Receiver
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check

D

DCP	Digital Communications Protocol
DID	Direct Inward Dialing
DLI	Digital Line Interface
DSP	Digital Signal Processor
DUCK	Data USART Clock

E

EIA	Electronic Industries Association
EMI	Electromagnetic Interference
EPF	Electronic Power Feed
EPROM	Erasable Programmable Read-Only Memory

H

HCMR	High Capacity Minirecorder

I

ID	Identification
INADS	Initialization and Administration System
I/O	Input/Output

L

LED	Light-Emitting Diode

M

MET	Multibutton Electronic Telephone
MO	Maintenance Object
Modem	Modulator-Demodulator
MPSC	Multi-Programmable Serial Controller

N

NMI	Non-Maskable Interrupt
NPE	Network Processing Element

P

PBX	Private Branch Exchange
PCM	Pulse Code Modulated
PDM	Processor Data Module
PIC	Programmable Interrupt Controller

R

RAM	Random-Access Memory
ROL	Readable Output Latch
ROM	Read-Only Memory
RTX	Real-Time Operating System

S

SAKI	Sanity and Control Interface
SAT	System Access Terminal
SMDR	Station Message Detail Recording
SPE	Switch Processing Element

T

TRIC	Transmit and Receive I-Channel Controller
TTR	Touch-Tone Receiver

U

USART	Universal Synchronous/Asynchronous Receiver and Transmitter

X

XACK	Transfer Acknowledge

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